IMPLEMENTATION OF DUAL DATA RATE-BASED SDRAM MEMORY FOR HIGH COVERAGE CONTROLLING USING HDL

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Abstract - Present days, DDR SDRAM (Double Data Rate Synchronous Dynamic Random-Access Memory) has become the most popular class of memory used in computers due to its high speed, burst access and pipeline feature. For high speed applications like image/video processing, signal processing, networking etc. DDR SDRAM is widely used. The basic operations of DDR SDRAM controller are similar to that of SDR (Single Data Rate) SDRAM; however, there is a difference in the circuit design; DDR simply use sophisticated circuit techniques to achieve high speed. To perform more operations per clock cycle DDR SDRAM uses double data rate architecture. DDR SDRAM (also known as DDR) transfers data on both the rising and falling edge of the clock. The DDR controller is designed with objective of proper commands for SDRAM initialization, read/write accesses, regular refresh operation, proper active and pre-charge command etc. DDR SDRAM controller is implemented using Verilog HDL and simulation and synthesis is done by using Xilinx ISE 14.5 accordingly.

KEY WORDS: DDR, SDRAM, BURST ACCESS, PIPELINE, VERILOG HDL

INTRODUCTION

Double data rate synchronous dynamic random-access memory (DDR SDRAM) is a class of memory integrated circuits used in computers. Nowadays, Memory devices are almost found in all systems, high speed and high-performance memories are in great demand. For better throughput and speed, the controllers are to be designed with clock frequency in the range of megahertz. As the clock speed of the controller is increasing, the design challenges are also becoming complex. Therefore, the next generation memory devices require very high-speed

controllers like double data rate and quad data rate memory controllers. With the rapid development in the processor's family, speed and capacity of a memory device is a major concern. The DDR is an enhancement to the traditional synchronous DRAM. The DDR is able to transfer the data on both the edges of each clock cycle. Thus, doubling the data transfer rate of the memory device. The DDR is available in a very low cost that's why it is widely used in personal computers where they are basically used to provide the functions of storage and buffers. The DDR SDRAM supports the data widths of 16, 32 and 64 bits. Its automatic refresh during the normal and power down modes. The DDR is a complete synchronous implementation of controller. It increases the throughput using command pipelining and bank management. This improvement allows the DDR module to transfer data twice as fast as SDRAM. As an example, instead of a data rate of 133MHz, DDR memory transfers data at 266MHz.DDR modules, like their SDRAM predecessors, arrive in there. Although motherboards designed to implement DDR are similar to those that use SDRAM, they are not backward compatible with motherboards that support SDRAM. You cannot use DDR in earlier SDRAM based motherboards, nor can you use SDRAM on motherboards that are designed for DDR.

Random access memory (RAM) is the best-known form of computer memory. RAM is considered "random access" because you can access any memory cell directly if you know the row and column that intersect at that cell. (RAM) data, on the other hand, can be accessed in any order. All the data that the PC uses and works with during operation are stored here. Data are stored on drives, typically the hard drives. However, for the CPU to work with those data, they must be read into the working memory storage (RAM).

Static Random-Access Memory uses a completely different technology. In static RAM, a form of flip-flop holds each bit of memory. A flip-flop for a memory cell takes four or six transistors along with some wiring, but never has to be refreshed. This makes static RAM significantly faster than dynamic RAM. However, because it has more parts, a static memory cell takes up a lot more space on a chip than a dynamic memory cell. Therefore, you get less memory per chip. Static Random-Access Memory uses multiple transistors, typically four to six, for each memory cell but doesn't have a capacitor in each cell. It is used primarily for cache. So static RAM is fast and expensive, and dynamic RAM is less expensive and slower. So, static RAM is used to create the CPU's speed-sensitive cache, while dynamic RAM forms the larger system RAM space.

DYNAMIC RANDOM-ACCESS MEMORY

Dynamic Random-Access Memory has memory cells with a paired transistor and capacitor requiring constant refreshing. DRAM works by sending a charge through the appropriate column (CAS) to activate the transistor at each bit in the column. When writing the row lines contain the state the capacitor should take on. When reading the sense amplifier determines the level of charge in the capacitor. If it is more than 50 percent, it reads it as a 1 otherwise it reads it as a 0. A memory chip rating of 70ns means that it takes 70 nanoseconds to completely read and recharge each cell. It is one of the most common types of computer memory (RAM). It can only hold data for a short period of time and must be refreshed periodically. DRAMs are measured by storage capability and access time. Storage is rated in megabytes (8 MB, 16 MB, etc.). Access time is rated in nanoseconds (60ns, 70ns, 80ns, etc.) and represents the amount of time to save or return information. With a 60ns DRAM, it would require 60 billionths of a second to save or return information. The lower the speed, the faster the memory operates. DRAM chips require two CPU wait states for each execution. Can only execute either a read or write operation at one time. The capacitor in a dynamic RAM memory cell is like a leaky bucket. It needs to be refreshed periodically or it will discharge to 0. This refresh operation is where dynamic RAM gets its name. Memory is made up of bits arranged in a two-dimensional grid. In which memory cells are fetched onto a silicon wafer in an array of columns (bit lines) and rows (word lines). The intersection of a bit line and word line constitutes the address of the memory cell. Memory cells alone would be worthless without some way to get information in and out of them. So, the memory cells have a whole support infrastructure of other specialized circuits. Identifying each row and column (row address select and column address select) Keeping track of the refresh sequence (counter) Reading and restoring the signal from a cell (sense amplifier) Telling a cell whether it should take a charge or not (write enable) Other functions of the memory controller include a series of tasks that include identifying the type, speed and amount of memory a checking for errors. The traditional RAM type is DRAM (dynamic RAM). The other type is SRAM (static RAM). SRAM continues to remember its content, while DRAM must be refreshed every few milliseconds.

DOUBLE DATA RATE SYNCHRONOUS DYNAMIC RANDOM-ACCESS MEMORY

Double Data Rate Synchronous Dynamic Random-Access Memory is the original form of DDR SDRAM. It is just like SDRAM except that is has higher bandwidth, meaning greater speed. Maximum transfer rate to L2 cache is approximately 1,064 MPs (for DDR SDRAM 133 MHZ). DDR RAM is clock doubled version of SDRAM, which is replacing SDRAM during 2001-2002. It allows transactions on both the rising and falling edges of the clock cycle. It has a bus clock speed of 100MHz and will yield an effective data transfer rate of 200MHz. DDR come in PC 1600, PC 2100, PC 2700 and PC 3200 DIMMs. A PC 1600 DIMM is made up of PC 200 DDR chips, while a PC 2100 DIMM is made up of PC 266 chips. Go for PC2700 DDR. It is about the cost of PC2100 memory and will give you better performance. DDR memory comes in CAS 2 and CAS 2.5 ratings, with CAS costing more and performing better.

DDR CONTROLLER ARCHITECTURE

The DDR SDRAM memory controller centre comprises of four primary hinders that are SDRAM controller, Control Interface, Command and Data Path Modules. The DDR SDRAM controller module is the best level module. That embodies three lower modules and unites the entire outline to give exact outcomes. The Control Interface module of SDRAM approaches summons and related memory addresses from the host and translating the charges and passing the look to the Command module. The Command module acknowledges summons and address from the Control Interface module for creating the correct orders to the SDRAM. The Data Path module handles the information way activities amid WRITE and READ orders. The best level module additionally instantiates two PPL's that are utilized as a part of CLOCK_LOCKS.

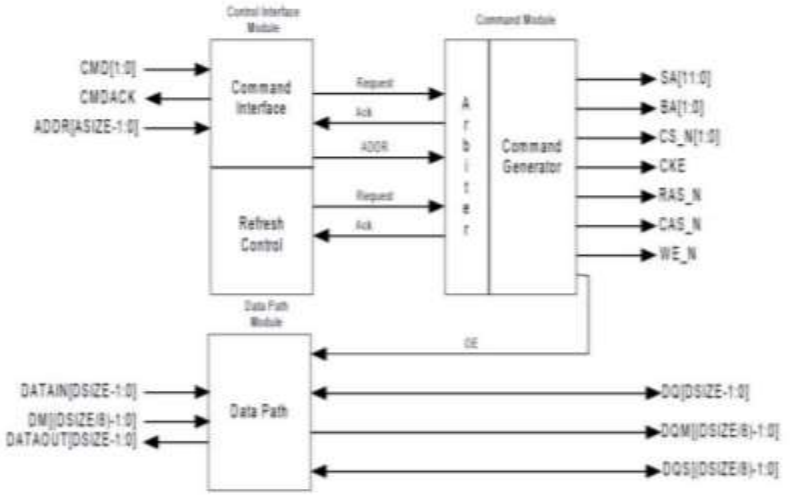

Figure 1: Functional Block Diagram of proposed DDR SDRAM Memory Controller core.

DDR SDRAM Control Interface Module The control Interface Module deciphers and registers charges from the host and tracks the decoded NOP, WRITEA, READA, REFRESH, PRECHARGE, and LOAD_MODE summons, alongside ADDR, to the Command Module. The LOAD_REG1 and LOAD_REG2 summons are decoded and utilized intramural to load the REG1 and REG2 registers with the qualities from ADDR. The Control Interface Module additionally contains a 16-bit down counter and control circuit that is utilized to generate periodic invigorate charges to the Command Module. A 16-bit down counter is stacked with the most noteworthy esteem of REG2 and checks down to zero. The REFRESH_REQ yield is cited with the counter achieves zero and remains cited until the point that the Command Module recognizes the demand. The recognize from the Command Module attaches the down counter to be reloaded with REG2 and the procedure rehashes. REG2 is a16-bit esteem that speaks to the period between REFRESH summons that the controller issues. The esteem is set by the condition int (REF_PERIOD/CLK_PERIOD).

DDR SDRAM Command Module The summon module gets decoded orders from the Control Interface Module, alongside invigorate demands from the revive control rationale and effectuates the suitable orders to the SDRAM. The module includes a basic referee that referees between the orders from the host interface and the invigorate demands from the revive control rationale. The invigorate supplications from the revive control rationale have need over the charges from the

host interface. On the off chance that a summon from the host appears in the meantime or amid a dormant revive task, the mediator holds off the host by not declaring CMDACK until the point when the inert invigorate activity is finished. On the off chance that a hid invigorate order is gotten while a host task is in advance then the concealed revive is held off until the point when the host activity is finished. After the authority has gained a charge from the host, the summon is passed onto the order generator segment of the Command Module. The summon Module utilizes three move registers to provoke the hopeful planning between the charges that are issued to the SDRAM. One move enlist is utilized to control the planning of the ACTIVATE summon while a moment moves enlist is utilized to control the situating of the READA or WRITEA charges and the third move enlist is utilized for timing order terms, all together for the judge to decide whether the last asked for task is finished. The Command Module likewise plays out the convolution of the address (ADDR) to the SDRAM. The column section of the deliver is multiplexed out to the SDRAM yields A [11:0] amid the ACTIVATE (RAS) charge. The section fragment is then multiplexed out to the SDRAM address yields amid a READA (CAS) or WRITEA charge.

DDR SDRAM Data Path Module One of the most difficult aspects of DDR SDRAM controller design is to transmit and capture data at double data rate. This module transmits data to the memories. The basic function of data path module is storing the write data and calculates the value for read data path. The Data Path Module issues the SDRAM information interface to the host. Host information is acknowledged on port DATAIN for WRITEA charges and information is given to the host on port DATAOUT amid READA commands. The information path width into the controller is twice the information way width to the DDR SDRAM gadgets. The information path module's DATAIN and DATAOUT ports are settled at 32bits and the DQ port is settled at 16bits. To construct data paths bigger than 32bits, Data Path Modules can be fell to expand the information transport width for increases of32bits. The DATAIN compose way takes the compose information and exchanges over to the CLK200 (two times the frequency of CLK100), multiplexing the information to the DQ port. On the read side, DATAOUT way, the read data is capture utilizing the flag CLK200 to test the information amid the centre of the information substantial window. The read data is demultiplexed and exchanged to the flag

CLK100 clock space, which is one a large portion of the recurrence of CLK200. The Data Path Module additionally creates the DQS motion amid compose tasks to the DDR gadgets. Data path module handles all the data generation and sampling task of DDR controller. For Read access, data is sampled by data path. Data is then synchronized with the internal clock and transferred to the user interface one-word per clock cycle as normal data rate. For Write access, data is received from the user interface at the normal one word per clock data rate. The DDR controller's data path then resynchronized the data and transfers them using the double data rate.

RESULTS

The design is simulated and synthesized on Xilinx ISE 14.5 accordingly. The simulation and synthesis results are shown in the following figures. The DDR SDRAM memory controller designed and analyzes the operations of read, write, auto precharge, precharge, no operation, mode register, load_register1 and load_register2 by using DDR SDRAM micron specifications. To test the main control module, initially the clock is given 100MHZ. The module will not be initialized until reset_n signal is made high. Once this signal is made high, it is necessary to make the delay signal (sys_dly_10us) high. This implies that the controller is provided with the necessary delay. After providing the delay signal, after some ns delay the controller gets initialized. This is indicated by the signal (sys_init_done) becoming high. Reset is made high and required system delay (10us) is given. Once the system gets initialized, the required data is written to the particular memory location. Now we can read the same data from memory.

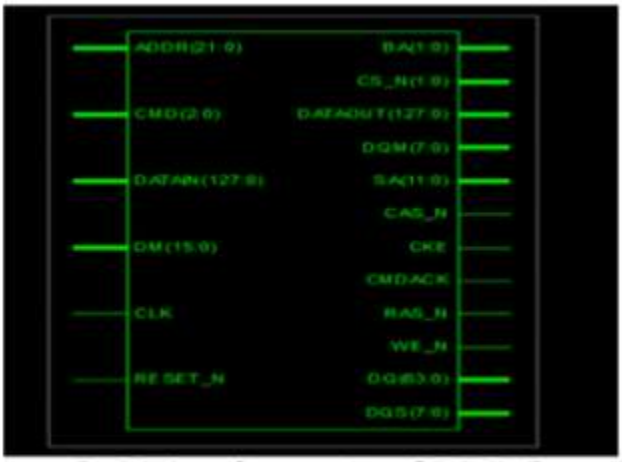

Figure 2: RTL schematic of DDR Controller

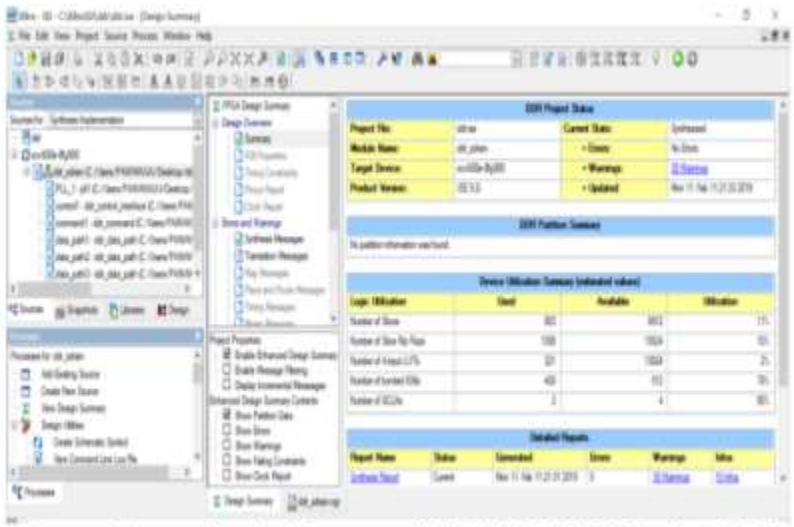

Figure 3: synthesis Report of DDR SDRAM Verilog HDL code.

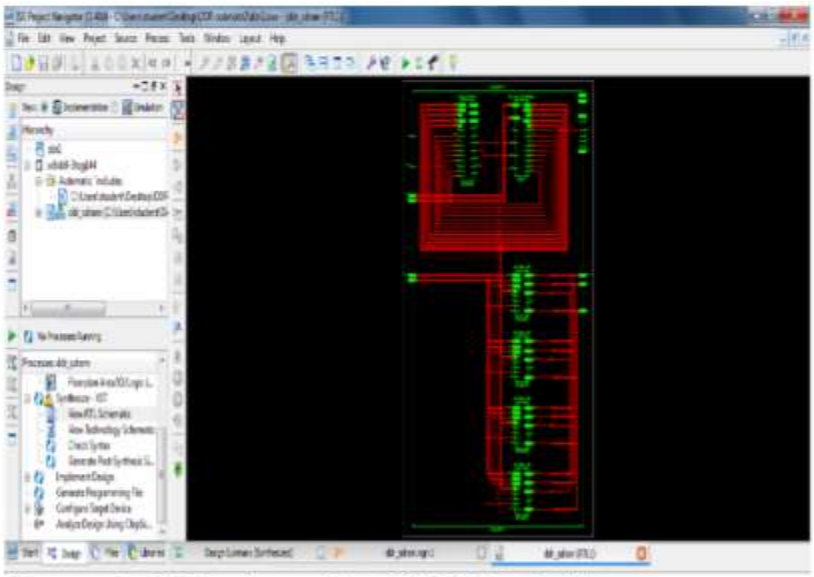

Figure 4: RTL schematic of DDR Controller

FIGURE 5: DDR SDRAM MEMORY CONTROLLER VERIFICATION WAVE FORM

CONCLUSIONS

In this paper an efficient fully functional DDR SDRAM controller is designed and verified by using Verilog HDL. The controller generates different types of timing and control signals, which synchronizes the timing and control the flow of operation. The memory system operates at double the frequency of processor, without affecting the performance. Thus, we can reduce the data bus size. The drawback of this controller is complex schematic with large number of buffers in the circuit increases the amount of delay.

FUTURE SCOPE: In the future studies, we will study how to reduce the cache leakage energy efficiently in a hybrid SPM and cache architecture. Since SPM can reduce the access frequency to the cache, we find it is possible to place the cache lines of the hybrid SPM-cache into the low power mode more aggressively than traditional leakage management for regular caches, which can reduce more leakage energy without significant performance degradation. Also, a Hybrid Drowsy-Gated Vdd (HDG) technique, which can adaptively exploit both short and long idle intervals to minimize leakage energy with insignificant performance overhead.

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