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Challan Recovery and Theft Vehicle Detection System

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ABSTRACT

Nowadays recovery of challan is a manual process which may leads to corruption and sometimes people will escape from paying it. And detection of stolen vehicles is also done manually by police department which takes more time and man power, so to counter these problems we have come up with a system "CHALLAN RECOVERY AND THEFT VEHICLE DETECTION SYSTEM". The purpose of this system is automatic recovery of pending Challan and identification of stolen vehicles with the help of radio frequency. A vehicle will hold an RFID tag. This tag is assigned with unique identification number by RTO or traffic governing authority. RFID Reader will be strategically placed at toll collection center. Whenever the vehicle which is having pending challan passes the toll collection center, the penalty amount will be deducted from his prepaid balance and displays the message on LCD. And also, the Reader verifies whether the vehicle details match with the details of stolen vehicle which were given by the police department. If the details are matched then BUZZER will be activated and toll gate will be closed.

I. INTRODUCTION

An embedded system is a special-purpose computer system designed to perform one or a few dedicated functions, sometimes with real-time computing constraints. It is usually embedded as part of a complete device including hardware and mechanical parts. In contrast, ageneral-purpose computer, such as a personal computer, can do many different tasks dependingon programming. Embedded systems have become very important today as they control many of the common devices we use.

Since the embedded system is dedicated to specific tasks, design engineers can optimize it, reducing the size and cost of the product, or increasing the reliability and performance. Some embedded systems are mass-produced, benefiting from economies of scale. Physically embedded systems range from portable devices such as digital watches and MP3 players, to large stationary installations like traffic lights, factory controllers, or the systems controlling nuclear power plants.

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Complexity varies from low, with a single microcontroller chip, to very high with multiple units, peripherals and networks mounted inside a large chassis or enclosure.

In general, "embedded system" is not an exactly defined term, as many systems have some element of programmability. For example, Hand held computers share some elements with embedded systems such as the operating systems and microprocessors which power them but are not truly embedded systems, because they allow different applications to be load and peripherals to be connected.

An embedded system is some combination of computer hardware and software, either fixed in capability or programmable, that is specifically designed for a particular kind of application device. Industrial machines, automobiles, medical equipment, cameras, household appliances, airplanes, vending machines, and toys (as well as the more obvious cellular phone and PDA) are among the myriad possible hosts of an embedded system.

Embedded systems that are programmable are provided with a programming interface, and embedded systems programming is a specialized occupation. Certain operating systems or language platforms are tailored for the embedded market, such as Embedded Java and Windows XP Embedded. However, some low-end consumer products use very inexpensive Challan Recovery and Theft Vehicle Detection System microprocessors and limited storage, with the application and operating system both part of single program

II.LITERATURE SURVEY

H.-I.Yang, et.al., [1] described “Impacts of NBTI/PBTI on timing control circuits and degradation tolerant design in nano scale CMOS SRAM,” IEEE Trans. Circuit Syst., vol. 58, no. 6, pp. 1239–1251, Jun. 2011.Negative-bias temperature instability (NBTI) and positive-bias temperature instability (PBTI) weaken PFET and NFET over the lifetime of usage, leading to performance and reliability degradation of nano scale CMOS SRAM. In addition, most of the state-of-the-art SRAM designs employ replica timing control circuit to mitigate the effects of leakage and process variation, optimize the performance, and reduce power consumption. NBTI and PBTI also degrade the timing control circuits and may render them ineffective. In this paper, we provide comprehensive analyses on the impacts of NBTI and PBTI on a two-port 8T SRAM design, including the stability and Write margin of the cell, Read/Write access paths, and replica timing control circuits. We show, for the first time, that because the Read/Write replica timing control circuits are activated in every Read/Write cycle, they exhibit distinctively different degradation behavior from the normal array access paths, resulting in degradation of timing control and performance. We also discuss

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degradation tolerant design techniques to mitigate the performance and reliability degradation induced by NBTI/PBTI.

S. Zafaret et.al.,[2] has discussed "A comparative study of NBTI and PBTI (charge trapping) in SiO2/HfO2 stacks with FUSI, TiN, Re gates," in Proc. IEEESymp. VLSI Technol. Dig. Tech. Papers, 2006, pp. 23–25. Threshold voltage (V_t) of a field effect transistor (FET) is observed to shift with stressing time and this stress induced V_t shift is an important transistor reliability issue. V_t shifts that occur under negative gate bias is referred as NBTI and those that occur under positive bias is referred as PBTI or charge trapping. In this paper, we present a comparative study of NBTI and PBTI for a variety of FETs with different dielectric stacks and gate materials. The study has two parts. In part I, NBTI and PBTI measurements are performed for FUSI NiSi gated FETs with SiO_2 SiO_2/HfO_2 and SiO_2/HfSiO as gate dielectric stacks and the results are compared with those for conventional SiON/poly-Si FETs. The main results are: (i) NBTI for SiO_2/NiSi and SiO_2/HfO_2/NiSi are same as those conventional SiON/poly-Si FETs; (ii) PBTI significantly increases as the Hf content in the high K layer is increased; and (iii) PBTI is a greater reliability issue than NBTI for HfO_2/NiSi FETs. In part II of the study, NBTI and PBTI measurements are performed for SiO2/HfO2 devices with TiN and Re as gates and the results are compared with those for NiSi gated FETs. The main results are: (i) NBTI for SiO_2/HfO_2/TiN and SiO_2/HfO_2/Re pFETs are similar with those observed for NiSi gated pFETs; and (ii) PBTI in TiN and Re gated HfO_2 devices is much smaller than those observed for SiO_2/HfO_2/NiSi. In summary for SiO_2/HfO_2 stacks, NBTI is observed to be independent of gate material whereas PBTI is significantly worse for FUSI gated devices. Consequently, HfO_2 FETs with TiN and Re gates exhibit over all superior transistor reliability characteristics in comparison to HfO_2/FUSI FETs

R.Vattikonda,et.al.,[3]"Modeling and minimization of pMOSNBTI effect for robust naometer design," in Proc. ACM/IEEEDAC, Jun. 2004, pp. 1047– 1052.Negative bias temperature instability (NBTI) has become the dominant reliability concern for nano scale PMOS transistors. In this paper, a predictive model is developed for the degradation of NBTI in both static and dynamic operations. Model scalability and generality are comprehensively verified with experimental data over a wide range of process and bias conditions. By implementing the new model into SPICE for an industrial 90nm technology, key insights are obtained for the development of robust design solutions: (1) the most effective techniques to mitigate the NBTI degradation are VDD tuning, PMOS sizing, and reducing the duty cycle; (2) an optimal VDD exists to minimize the degradation of circuit performance; (3) tuning gate length or the switching frequency has little impact on the NBTI effect; (4) a new switching scenario is identified for worst case timing analysis during NBTI stress

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S. Zafar, et.al,[4] has told that"Thresh-old voltage instabilities in high-k gate dielectric stacks," IEEE Trans. Device Mater.Rel., vol. 5, no. 1, pp. 45–64, Mar. 2005. An experimental and modeling study of charge trapping related threshold voltage shifts in Al2O3 and HfO2 *n*-type field effect transistors (nFET) is reported. The dependence of threshold voltage, subthreshold slope, and gate leakage currents on stressing time and injected charge carrier density are investigated as a function positive bias stress voltage and temperature. Based on experimental data, a model for trapping of charges in the existing traps is developed. The model is similar to SiO2 charge trapping models with one exception. Unlike SiO2 models, the model assumes a continuous distribution in trapping capture cross sections. The model predicts that threshold voltage would increase with a power law dependence on stressing time and injected charge carrier density (Ninj) in the initial stages of stressing. The model calculates threshold voltage shifts as a function of stress time and *N*inj, thereby provides estimates of threshold voltage shifts after 10 years lifetime. It also provides insights into the nature of traps by estimating trapping capture cross sections. The calculated results are shown to be consistent with both Al2O3 and HfO2 data over several decades of stressing time and *N*inj. Using the model, a comparison between Al2O3 and HfO2 is made. In addition, the model is compatible with charge trapping data reported by other research groups.

H. Abrishami, et.al,[5] described "NBTI-aware flip-flop characterization and de-sign," in Proc. 44th ACM GLSVLSI,2008, pp. 29–34 With the scaling down of the CMOS technologies, Negative Bias Temperature Instability (NBTI) has become a major concern due to its impact on PMOS transistor aging process and the corresponding reduction in the long-term reliability of CMOS circuits. This paper investigates the effect of NBTI phenomenon on the setup and hold times of flip-flops. First, it is shown that NBTI tightens the setup and hold timing constraints imposed on the flip-flops in the design. Second, different types of flip-flops exhibit different levels of susceptibility to NBTI-induced change in their setup/hold time values. Finally, an NBTI-aware transistor sizing technique can minimize the NBTI effect on timing characteristics of the flip-flops.

S. V. Kumar, et.al., [6] has told that"NBTI-aware synthesis of digital circuits," in Proc. ACM/IEEE DAC, Jun. 2007, pp. 370–375.Negative bias temperature instability (NBTI) in PMOS transistors has become a major reliability concern in nanometer scale design, causing the temporal degradation of the threshold voltage of the PMOS transistors, and the delay of digital circuits. A novel method to characterize the delay of every gate in the standard cell library, as a function of the signal probability of each of its inputs, is developed. Accordingly, a technology mapping technique that incorporates the NBTI stress and recovery effects, in order to ensure optimal performance of the circuit, during its entire lifetime, is presented. Our technique, demonstrated over 65 nm benchmarks

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shows an average of 10 % area recovery, and 12 % power savings, as against a pessimistic method that assumes constant stress on all PMOS transistors in the design.

A. Calimera, et.al.,[7] described "Design tech-niqures for NBTItolerant power- gating architecture," IEEE Trans. Circuits Syst., Exp.Briefs, vol. 59, no. 4, pp. 249–253, Apr. 2012.The main constraint in VLSI system design is to achieve low power devices. In any digital filter, multipliers are the major elements. The throughput is the major parameter of multiplier that influences the performance of multiplier. For long term usage, aging becomes the main constraint that affects the performance of the system. Majorly aged systems fail due to delay problems. There are many approaches to design multipliers that reduce this aging effect. But these systems require large area, power. Moreover, timing violations occur when fixed latency designs are used. For reducing these timing violations and for implementing an aging reliable low power multiplier, adaptive hold logic is used. The transistor speeds are influenced by both negative and positive bias temperatures, for long term applications due to aging effect, the system may fail to perform because of timing violations. Therefore, it is necessary to implement the high performance designs. Here we propose a reversible Wallace Tree multiplier design with razor flip flop based multiplier circuit. This design is able to provide high throughput for area power critical applications. The proposed method can be digital filters to enhance the performance in the real time environment.

K.-C. Wu et.al.,[8] has described "Joint logic restructuring and pin reordering against NBTI-induced performance degradation," in Proc. DATE,2009, pp. 75–80.Negative Bias Temperature Instability (NBTI), a PMOS aging phenomenon causing significant loss on circuit performance and lifetime, has become a critical challenge for temporal reliability concerns in nanoscale designs. Aggressive technology scaling trends, such as thinner gate oxide without proportional downscaling of supply voltage, necessitate a design optimization flow considering NBTI effects at the early stages. In this paper, we present a novel framework using joint logic restructuring and pin reordering to mitigate NBTI-induced performance degradation. Based on detecting functional symmetries and transistor stacking effects, the proposed methodology involves only wire perturbation and introduces no gate area overhead at all. Experimental results reveal that, by using this approach, on average 56% of performance loss due to NBTI can be recovered. Moreover, our methodology reduces the number of critical transistors remaining under severe NBTI and thus, transistor resizing can be applied to further mitigate NBTI effects with low area overhead.

III .EXISTING SYSTEM & PROPESED SYSTEM

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EXISTING SYSTEM

Nowadays recovery of pending challan is a manual process, which requires more time and man power. If a vehicle passing through the toll collection centre , then police department needs to check whether that vehicle has pending challan or not manually by using hard copies of data or they need to check in some e challan apps in mobile phone by entering the vehicle details.

In case of identification of stolen vehicles, the existing system comes with lots of flaws and some unmanageable circumstances, which is inefficient most of the time. Police department identifies these vehicles by using number plate and some other bike details. In some cases the burglar can change the number plate which leads to manipulation of police. The maintenance of hard copy of all the documents and the need of carrying for verification adds to daily hectic of life.

LIMITATIONS

▪ By this manual process we can recover the challan but it takes more time and sometime leads to corruption and also few people escape from paying it.

▪ May cause disturbances in traffic as vehicle needs to be in queue for long time also consumes more fuel.

▪ Manual identification of stolen vehicles is very hectic job requires more man power.

▪ This will leads to raise in crime such as traffic violations and theft of vehicles.

PROPOSED SYSTEM

OBJECTIVES

• To recover the pending challans automatically at toll collection centers using RFID technology.

• To detect the stolen vehicles at toll gates which saves more time and effort.

• To reduce crimes such as theft of vehicles and traffic rules violation

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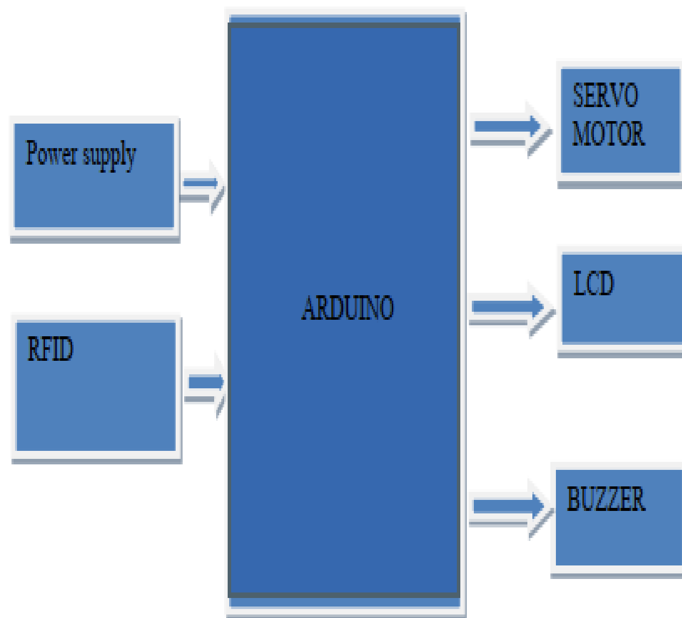

Fig 3.1 BLOCK DIAGRAM

WORKING:

The primary concept of our system is that every vehicle will hold an RFID tag. This tag is assigned with unique identification number by RTO or traffic governing authority. In accordance with this number, we will store all basic information as well as the amount he has paid in advance for the TOLL collection. RFID Reader will be strategically placed at toll collection center. Whenever the vehicle which is having pending challan passes the toll collection center, the penalty amount will be deducted from his prepaid balance. New balance will be updated. In case if one has insufficient balance, his updated balance will be negative one. To tackle this problem, we are alarming a sound, which will alert the authority that this vehicle doesn't have sufficient balance and that vehicle can be trapped.

The Reader verifies whether the vehicle details match with the details of stolen vehicles which were given by the police department. Whenever the theft of vehicle takes place then vehicle owner will raise a complaint in police station which includes basic information and particular RFID number at police station. These details are sent to Toll collection centers and the data will be updated daily at end of the day.

IV.RESULT & DISCUSSION

In this way system will automatically recover penalty for violation of traffic rules and in turn will lead to a disciplined traffic in our country. It will help in minimizing many problems related to traffic which brings disturbance to the whole system and will help in reducing number of accidents; traffic jam which consumes our precious time and also reduces the theft of vehicles

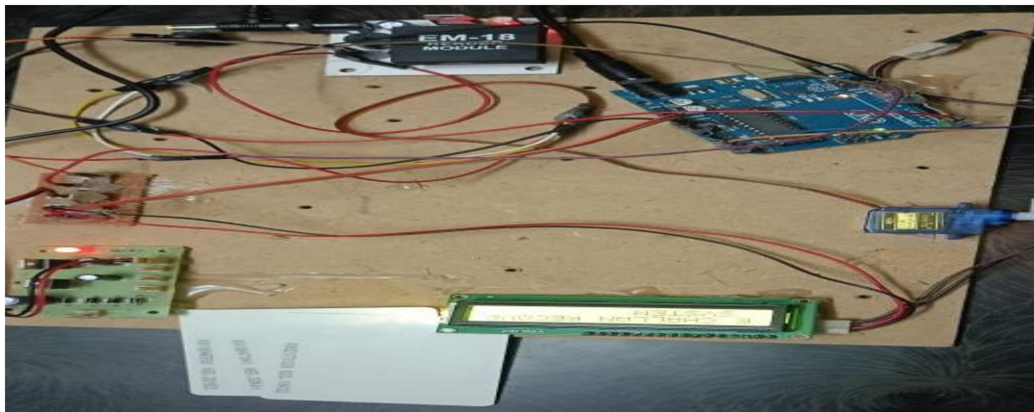

FIG 1.0 HARDWARE KIT RESULT

REFERENCES

[1] H.-I. Yang, S.-C.Yang, W. Hwang, and C.-T. Chuang, "Impacts of NBTI/PBTI on timing control circuits and degradation tolerant designinnanoscale CMOS SRAM," IEEE Trans. Circuit Syst., vol. 58, no. 6, pp. 1239–1251, Jun. 2011.

[2] S. Zafaret al., "A comparative study of NBTI and PBTI (charge trapping) in SiO2/HfO2 stacks with FUSI, TiN, Re gates," in Proc.IEEESymp. VLSI Technol. Dig. Tech. Papers, 2006, pp. 23–25.

[3] R.Vattikonda,W.Wang,andY.Cao,"ModelingandmiimizationofpMOSNBTIeffect for robust naometer design," in Proc. ACM/IEEEDAC, Jun. 2004, pp. 1047– 1052.

[4] S. Zafar, A. Kumar, E. Gusev, and E. Cartier, "Thresh-old voltage instabilities in high-k gate dielectric stacks," IEEE Trans. Device Mater.Rel., vol. 5, no. 1, pp. 45–64, Mar. 2005.

[5] H. Abrishami, S. Hatami, B. Amelifard, and M. Pe-dram, "NBTI-aware flip-flop characterization and de-sign," in Proc. 44th ACM GLSVLSI,2008, pp. 29–34

[6] S. V. Kumar, C. H. Kim, and S. S. Sapatnekar, "NBTI-aware synthesis of digital circuits," in Proc. ACM/IEEE DAC, Jun. 2007, pp. 370–375.

[7] A. Calimera, E. Macii, and M. Poncino, "Design tech-niqures for NBTItolerant power-gating architecture," IEEE Trans. Circuits Syst., Exp.Briefs, vol. 59, no. 4, pp. 249–253, Apr. 2012.

[8] K.-C. Wu and D. Marculescu, "Joint logic restructur-ing and pin reordering against NBTI-induced perfor-mance degradation," in Proc. DATE,2009, pp. 75–80.