Design and Implementation of LPC: An Error Correction Code to Reduce Errors in Three Dimensional(3D) Memories on FPGA

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Abstract In this project, Reliability of memories has been problematic when CMOS manufacturing technology scales down because memory cells' radiation sensitivity increases rapidly. The advantages of 3D technology over 2D technology have drawn attention. These advantages include high integration density, high performance, low power consumption, and fast communication speed. Despite the fact that 3D memory are the subject of numerous studies, little research has been done on how this technology affects reliability. To create dependable 3D memory, this project presents Line Product Code (LPC), a modified version of the product code-based Error Correction Code (ECC) that makes use of parity in both rows and columns as well as Hamming. We developed two LPC-based decoding algorithms that are lightweight and can be used in both interleaved (LPCa-I) and non-interleaved (LPCa) variants. This allowed us to examine LPC using a set of simulated instances that consider four different levels of error incidence severity. The LPC-based algorithms were found to be more effective than other Hamming-based algorithms in the experimental results, with correction rates up to 2.3 times higher.

Keywords: LPC(Low Parity Check),6G Communications, FPGA, Verilog HDL, ECC and ECE.

I.INTRODUCTION

The market demand for complex applications boosts researches on CMOS manufacturing technologies that carried a significant reduction in the transistor size [1]. In turn, the transistor scaling down contributes to the increase of temporary faults in electronic elements, such as memories, whose content modification may cause a wrong execution of programs that may not be tolerated in some cases [2]. These faults have been studied for over 40 years [3]-[6] and are classified as Single-Event Upset (SEU), Multiple-Cell Upsets (MCU), and Multiple-Bit Upsets (MBU). SEU occurs in a single cell while an MCU arises in more than one cell; finally, an MBU happens when an MCU occurs in the same logical word [7]. There are several techniques for mitigating these faults in electronic devices, such as improving the process technology, using hardened memory cell, Triple Modular Redundancy (TMR) or Error Correction Code (ECC). To minimize faults, Silicon on Insulator (SoI) technology uses a thin layer of silicon on top of the insulator during the chip manufacturing process. In the hardened memory cell approach, some circuits are replaced by their hardened versions, which are less susceptible to faults but consuming more area and implying more latency. The TMR technique uses three identical implementations of the same logic function, and the outputs are connected to a voter that decides mostly the correct result [8]. Lastly, the ECC basic concept is to have an encoding and decoding algorithm for restoring the correct value of the information placed in a memory cell or

transmission channel [9]. The evolution of manufacturing technology reaches significant reductions in Two-Dimensional (2D) memories, increasing the challenges to reach reliable circuits [1]. Recently, Three-Dimensional (3D) integration technology, which enables multi-layer stacking, has attracted attention – Section 3 gives some recent works targeting reliability on 3D devices. The advantages of 3D technology include high integration density, high performance, low power dissipation, and high on-chip communication speed [10]-[17]. Section 2 describes another advantage of the 3D integration technologies - stacking several dies on top of each other suggests that incident particles must penetrate multiple layers of material before reaching transistors on the inner layers. Thus, stacked dies can block some particles before reaching deeper layers of the 3D chip, changing the Soft Error Rate (SER) at different 3D chip dies [2]. This stacking effect on SER is one of the essential points that this paper regards to evaluate the ECCs capacity. This work also addresses the problem of chip warming; especially for 3D memories placed on the top of the active logic, the bottom layer of the memory is the most exposed to heat dissipation, making the bottom layer in 3D memory hotter than the top ones. Heat is another source of transient errors, and the heat profile in 3D memory provides varying degrees of reliability for each layer. From a heat perspective, the upper dies are less susceptible to errors, forming a different SER distribution in 3D memory [13]. Besides, the performance benefits and thermal impact of the stacked 3D microarchitecture have been studied recently, but the reliability implications and the MBU patterns when using 3D technology have received little attention. The novelty of this work is to propose the Line Product Code (LPC), a new product-type ECC, to increase the correction rate and reliability of 3D memories. LPC is a lighter ECC that does not employ the redundancy overhead of the straightforward product codes, providing a decoding algorithm elaborated to achieve a high error correction rate. decoding algorithms based on LPC - LPCa and LPCa-I, which are non-interleaved and interleaved versions. Besides, we described two other ECC configurations used in the analysis of this work. Section 5 explains how the organization of LPC is mapped on a physical memory. Section 6 presents the experimental results with the test sequence and an MBU generation algorithm, which is suitable to represent faults on 3D memories. Section 7 demonstrates that the LPCa-based algorithms achieve high error correction rates and are suitable for use in applications where reliability is a critical requirement, such as in space applications. Besides, Section 7 includes the results and discussions based on code correctability, reliability, and computational cost.

Due to the physical structure of 3D technologies, the upper layers protect the lower ones from high energy particles. Zhang and Li [2] analyze SERs for 3D-ICs based on the effect of alpha particles emitted from the decay of radioactive impurities in the interconnect metallization and package material. The authors state that the flux of alpha particles generated from the Integrated Circuit (IC) plastic packaging material is almost ten times greater than that of the metallization layers, and the metallization layers block more than 30% of these particles before reaching an active layer; besides, only 0.4% of the particles can reach the active layer of a second die from the top. Thus, the lower layers of a 3D memory have lower error rates than the higher ones, which is an advantageous feature of 3D technologies [12][13][17][18].

Additionally, high temperature is another source of transient errors, and the stacked architecture causes a heating problem since the lower layers of memory are less exposed to the heat dissipation, making them warmer more than the upper layers; thus, the heat profile in 3D memory provides different degrees of reliability for each layer. From a heat perspective, this

makes the lower dies more susceptible to errors, forming an unequal distribution of SER through the 3D layers [13][18].

Han, Chung, and Yang [13] used both the effect of radation and heat to produce a model of equations to estimate SER among the layer levels of a 3D-IC. Figure 1 depicts four test cases created by the authors using these equations: (a) SER of the uppermost layer is 10× higher than the other layers. This case is based on the analysis introduced in [2], which only considers the effect of alpha particles strike on the top layer, (b) SER is 5× higher than the others since the flux of alpha particles is reduced, (c) SER of the first and second layers are respectively 10× and 5× higher than the other layers, and (d) SER of the uppermost and lowermost layers are 10× higher than the others. This case regards the strike of alpha particles and the heat dissipation from an active layer bellow the stacked memories.

There are some works that investigate reliability issues on 3D devices. For instance, Bagatin et al. [14] investigated the sensitivity of 3D NAND flash memories to wide-energy spectrum neutrons. The effects of neutron exposure were studied in terms of threshold voltage shifts and raw bit error rates; they extrapolated the neutron failure rates obtained in the accelerated tests to field conditions at sea level and aircraft altitudes. Kim and Yang [18] proposed a reliability structure for reducing faults on the bits, which considers asymmetric SERs per layer in a 3D die-stacked memory using a deep neural network. Their experimental results demonstrate that the proposed method improves fault tolerance regardless of the model type.

The works [1] and [15] also focus on 3D NAND flash memories. Bagatin et al. [1] investigated the effects of heavy-ion irradiation on 3D memory cells; threshold voltage distributions are studies before and after exposure, as a function of the irradiation angle. The same authors investigated in [15] the effects of total ionizing dose on 3D memories irradiated with gamma rays.

Finally, we describe three works that analyze ECCs targeting 3D memories. Han, Chung, and Yang [13] proposed a novel ECC organization scheme for 3D memories to secure reliable operations under SER profiles. The proposed scheme does not require additional redundant arrays. Instead, it employs unused spare columns of relatively reliable layer memories to store additional check-bits of less reliable layer memories. Chang, Huang, and Li [17] proposed an area and reliability efficient ECC scheme for 3D RAMs, taking advantage of the shielding effect. Han and Yang [12] introduced a 3D memory scheme to ensure reliable operations by enhancing the ECC capacity of upper layer memories. Experimental results show that the proposed method can tolerate more than three times the bit.error rate than the conventional method. These three papers introduce new ECC configurations in 3D components, but there is no standard in how to present the results. Our work focuses on the presentation through three metrics: ECC correctability, hardware cost analysis, and system reliability. Besides, this work introduces a methodology to generate synthetic upsets considering radiation and heat effects on 3D devices.

II.EXISTING SYSTEM AND PROPOSED SYSTEM

1.EXISTING SYSTEM: LPC-based Decoding Algorithm

The decoding algorithm can explore full code potentialities or implement a more lightweight version to reduce synthesis costs. This work introduces LPCa and LPCa-I, two LPC-based decoding algorithms in non-interleaved and interleaved versions, respectively. Both LPC-based algorithms have the same correction method that explores double and single error knowledge to perform a heuristic technique that reaches high error correction rates, without increasing a lot the implementation cost of the decoding algorithm. LPCa and LPCa-I differ only on the codeword organization into the target memory.
It appears that you are referring to the implementation of two lightweight decoding algorithms based on (LPC) codes. Specifically, these algorithms are designed for decoding in interleaved (LPCa-I) and non-interleaved (LPCa) configurations. Let's break down the key elements:

1. (LPC) Codes:
LPC codes are a class of error correction codes used in coding theory. They are known for their ability to provide efficient error correction while having a sparse parity-check matrix, contributing to lower decoding complexity.

2. Lightweight Decoding Algorithms:
Lightweight decoding algorithms are designed to provide efficient and low-complexity decoding processes. This is particularly important in resource-constrained environments, such as embedded systems or low-power devices.

3. Interleaved (LPCa-I) and Non-Interleaved (LPCa) Configurations:
Interleaving is a technique used in error correction codes where bits are rearranged before transmission to improve error correction performance. Interleaved decoding algorithms handle the decoding of interleaved codes. Non-interleaved codes, on the other hand, do not use interleaving.

4. Implementation:
Implementing lightweight decoding algorithms involves translating the algorithmic steps into actual code that can run on a computing system. The specific details of the implementation will depend on the chosen programming language, hardware platform, and the characteristics of the LPC codes being used.

Possible Steps in the Implementation:
Matrix Representation: Convert the LPC codes into matrix representations, particularly the parity-check matrix, which is sparse in the case of LPC codes.
Decoding Logic: Implement the decoding logic based on the chosen algorithm. This could involve methods like belief propagation, message passing, or other decoding techniques suitable for LPC codes.
Interleaving/Deinterleaving: For the interleaved version (LPCa-I), include logic for interleaving and deinterleaving of the codewords before and after transmission.
Optimization: Ensure that the algorithms are optimized for lightweight and efficient operation, considering constraints such as memory usage, computational complexity, and power consumption.

Testing:

Thoroughly test the implemented algorithms using various test cases and scenarios to validate their correctness and performance.
These codes are a class of error correction codes that have gained significant attention due to their excellent error correction performance.

2.PROPOSED SYSTEM

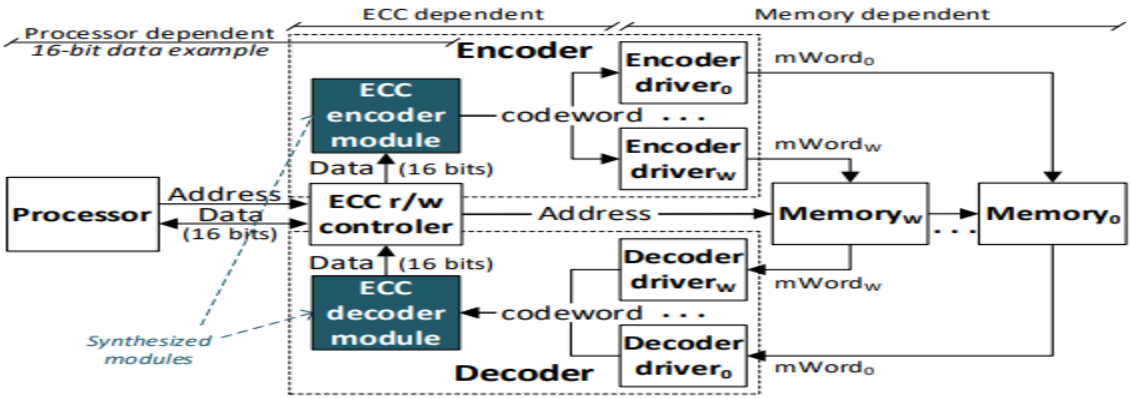

Figure 1. proposed LPC encoding/decoding flow describing the modules that depend on the processor, ECC, and memory characteristics.

The LPC described in this project was implemented to be used in 16-bit memories, the size of memory used in the experimental results section. However, the coding model defined by LPC can be applied to memories with different manufacturing technologies, sizes, formats, and protocols, as it implements a coding layer that can be adapted to different types of reading and writing procedures in memory. For example, a logical organization of 32-bit memory words can be implemented employing LPC with two 16- bit data codes (i.e., 2×48 bits). Considering this example, the processor would only have one access for writing or reading, and the subsequent level implemented by an encoder/decoder adjusts the physical memory requirements. In this same example, assuming a physical memory with 32-bit words, three writes/readings to/from physical memory is needed to access the 96 bits required by the two LPC codewords. In this case, the encoder/decoder is responsible for converting the physical and logical words. Figure 11 illustrates the encoding and decoding schemes considering various types of memories with specific reading and writing drivers to clarify the synthesized modules. It is important to note that while the ECC encoder and decoder modules are only dependent on the processor address/data size and ECC algorithms, the driver modules are memory configuration dependents. mWordW mWord0 . . . mWordW mWord0 ECC dependent Memory dependent Synthesized modules Processor Data (16 bits) Address Memory0 . . . Decoder driverW Decoder Decoder driver0 . . . Encoder driver0 Encoder driverW Encoder MemoryW ECC encoder module ECC decoder module Address ECC r/w controler Processor dependent 16-bit data example Data (16 bits) codeword codeword Data (16 bits) Figure 1. LPC encoding/decoding flow describing the modules that depend on the processor, ECC, and memory characteristics. Additionally, the 3D fault model makes room for the codeword to be addressed in multiple layers; this is because different paths have different rates of error incidences. Thus, the distribution of a word in more than one memory layer increases the probability of having fewer errors within the codeword and, consequently, more decoding success. Another opportunity is to use LPC in layers more

susceptible to faults, such as the upper and lower memory layer, and use less robust ECCs (therefore, with a lower associated cost) in layers less susceptible to bitflips. Finally, we point out that LPC can even be used as the standard for memories that require a high degree of reliability and employ ECC on-die [34][35], as in this case, the ECC becomes transparent to the memory controller. Implementing an on-die ECC allows the complete knowledge of the physical organization of the memory bits; this knowledge makes it possible to apply codes that implement, for example, interleaving techniques, further increasing the ability to correct bitflips concentrated in a memory neighborhood.

III. RESULTS AND ANALYSIS DISCUSSION

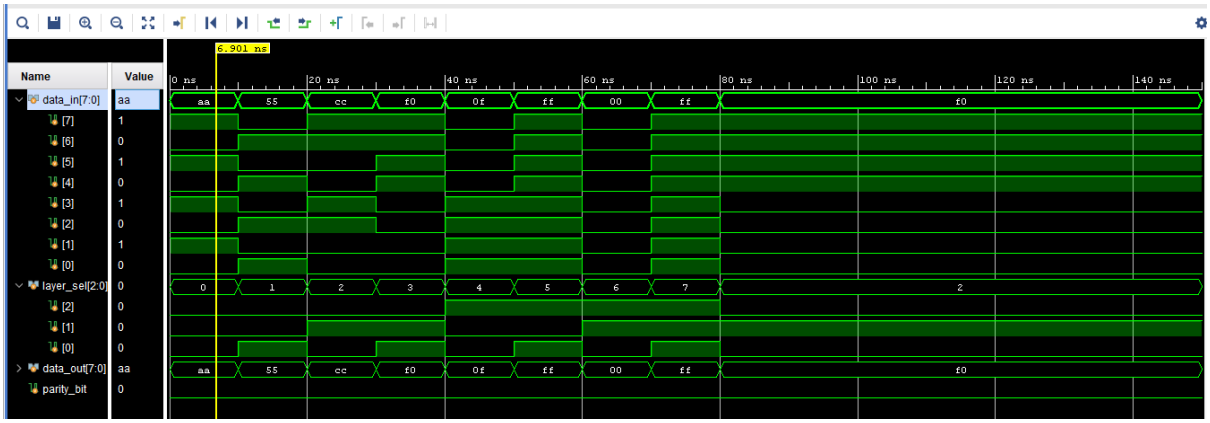

FIG.1.LPC SIMULATED OUTPUT

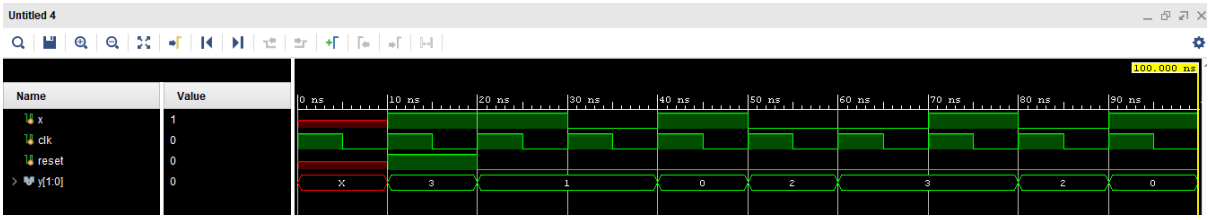

FIG.2.ENCODER OUTPUT

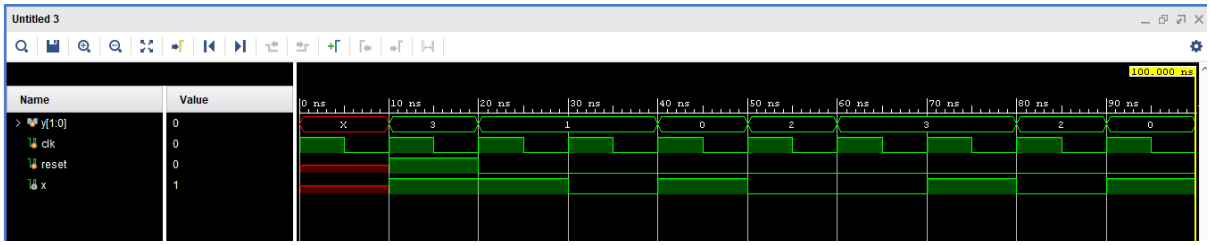

FIG.3.DECODER OUTPUT

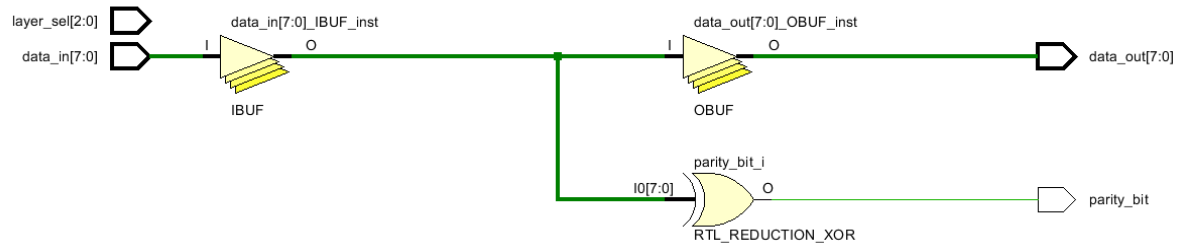

FIG.4.LPC RTL SCHEMATIC DIAGRAM

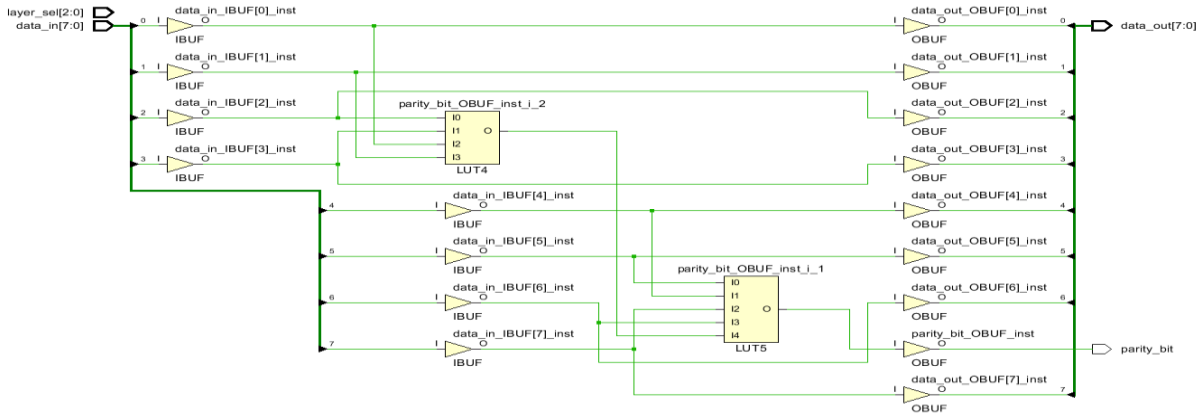

FIG.5.LPC SYNTHESIS DESIGN

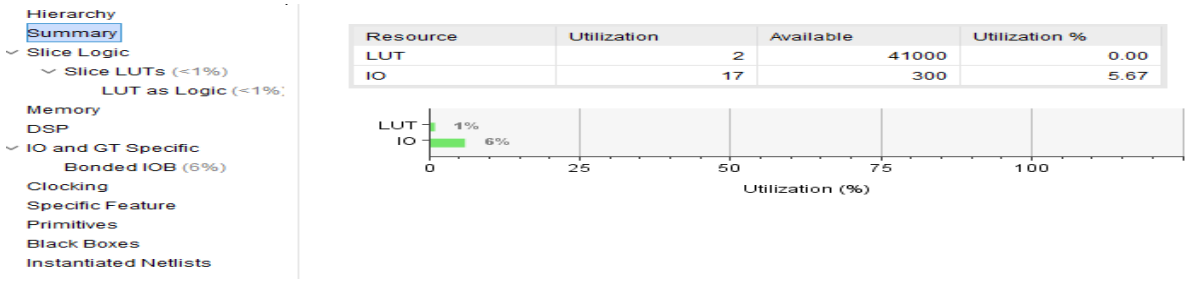

FIG.6.UTILIZATION REPORT OF LUTS AND AREA

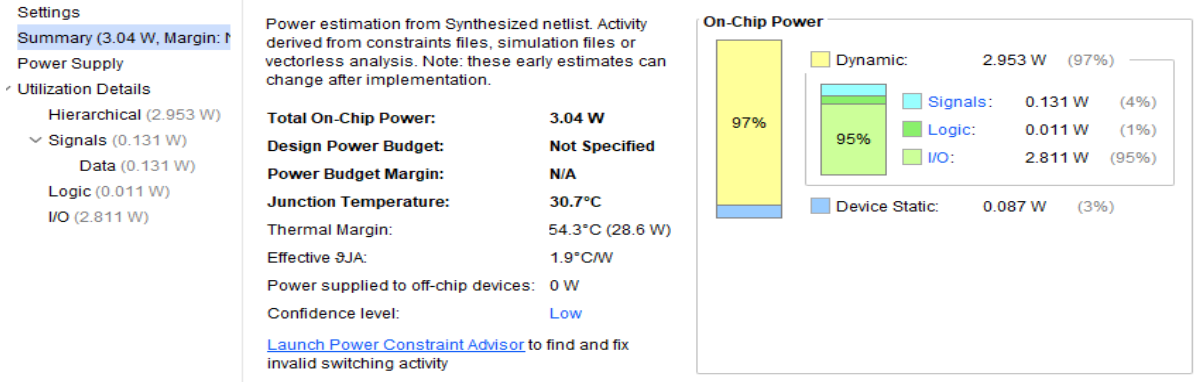

FIG.7.POWER REPORT

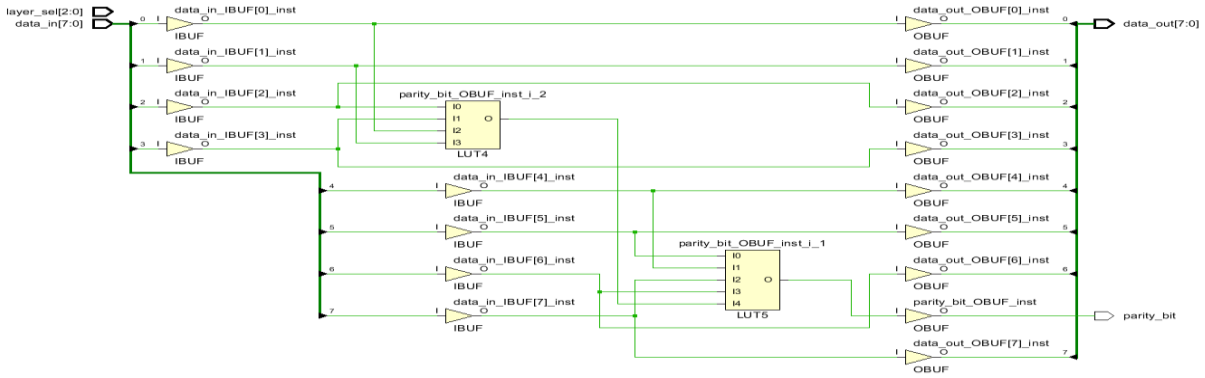

FIG.8.LPC IMPLEMENTAED AND OPTIMIZED DESIGN

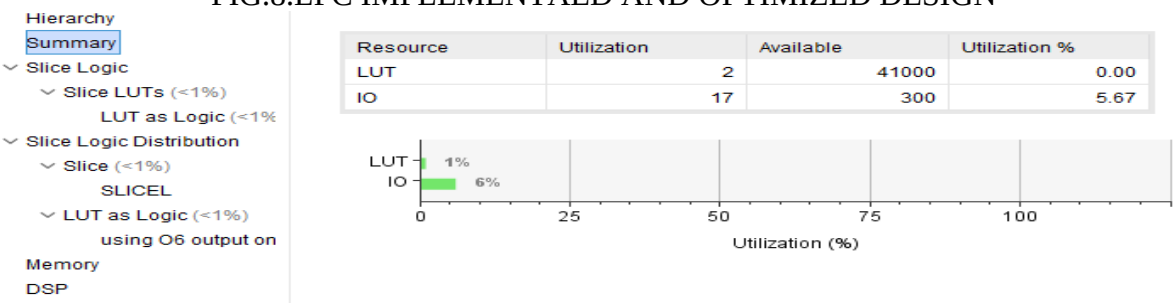

FIG.9.LPC UTILIZATION REPORT

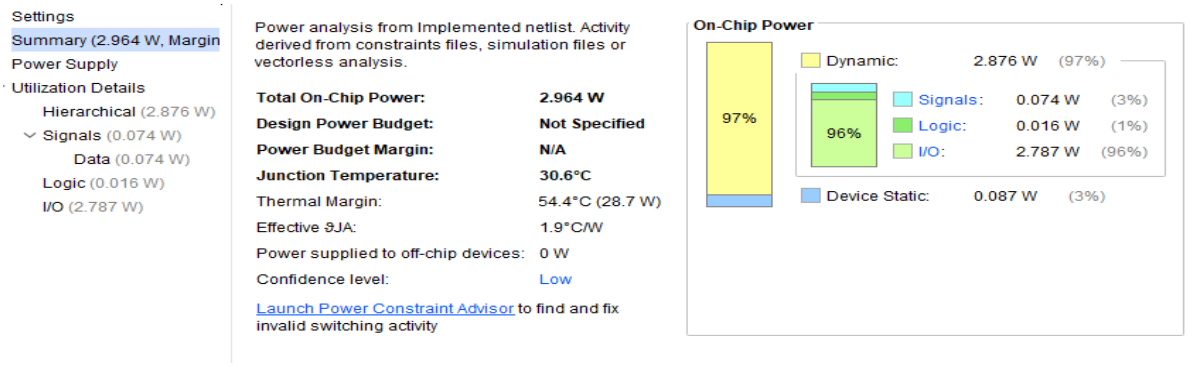

FIG.10.OPTIMIZED LPC DESIGN POWER

Conclusion

This work proposes LPC - a product-type ECC that uses Hamming and parity codes on both rows and columns. The experimental results demonstrate that this code implemented in two lightweight decoding versions, in interleaved (LPCa-I) and non-interleaved (LPCa) algorithms, has high error correction capability enabling its usage in space application memories. The validation of the proposed ECC and the correction technique applied by the LPCa-based decoding algorithms were performed using a set of simulations varying the error severity level and test cases, producing different numbers of errors on the dies of the 3D memory.

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