DESIGN AND IMPLEMENTATION OF PHASE INTERPOLATION IN ANALYTICAL MODELING OF JITTER IN BANG-BANG CDR CIRCUITS

Mr.K.Ch.Malla Reddy[(1)] Mr.A.Prasad[(2)] Shaik Intiyaz[(3)] Anumula Anil Kumar[(4)] Duddela Mahendra Reddy[(5)] Grandhi Krishna Mahesh[(6)]

[1,2] *Krishna Chaithanya Institute Of Technology & Sciences, Ece Department, Markapur, Andhra Pradesh.*

[3,4,5,6,] *Krishna Chaithanya Institute Of Technology & Sciences, UG Student-ECE, Markapur, Andhra Pradesh.*

Abstract In this paper, compact expressions for the jitter in clock and data recovery (CDR) circuits based on bang-bang phase detectors are proposed. These expressions consider the quantization noise related to the finite number of phases of the phase interpolator (PI), which aligns the receiver clock to the incoming data, as well as the phase noise of the transmitter and receiver oscillators. Various methods for detecting edges and deserialized data using Early/Late detection are compared. Majority voting reduces CDR bandwidth and amplifies the effect of clock jitter on CDR jitter; counting individual Early/Late occurrences, on the other hand, does not reduce bandwidth but does increase noise associated with the PI's finite phases. Validation of the suggested analytical results are simulated in Xilinx Vivado verilog Hdl.

Keywords: Jitter and Bang Bang Circuits,5G Communications, FPGA, Verilog HDL,LT-Spice.

I.INTRODUCTION

The increasing demand for high-speed I/O in electronic systems has pushed the development of high-speed serial interfaces operating at rates up to 112 Gb/s [1]. Among the different clocking strategies [2], the use of embedded clock results in pin and power saving but requires clock and data recovery (CDR) systems to align the receiver clock to the received data [3]. The alignment is usually performed with a phase interpolator (PI) that derives a set of discrete phases from the receiver clock [4]. The use of bang-bang phase detectors based, e.g., on the Alexander algorithm [5] makes the CDR system essentially digital [6], [7].

Being the combination of different subblocks, the design of a CDR circuit should start from system-level considerations before actually placing and sizing the single transistors. In this respect, system-level modeling plays an important role in the initial design phase. Although faster than circuit-level analysis, time-domain behavioral simulations [8] still require a level of detail that is not needed in the very initial phase of the system planning. For this reason, simple analytical formulas can serve as a starting point to set the main specs of the system.

Linearization of the bang-bang characteristic is the first step to derive analytical formulas for the CDR system [9]–[12]. Having as a target the estimate of the output jitter, a linear model can be

used to compute the effect of the single noise sources on the overall jitter. A summary of the main approaches proposed in the literature is provided in [16]. Most of the works focus on the linearization of the phase detector and on the inclusion of loop delay (latency). However, in digital phase-locked loop (PLL) and digital CDR other blocks feature quantization effects: [13] includes the quantization error of the digitally controlled oscillator (DCO) in a linearized PLL model.

In this paper, we extend the analyses available in the literature by considering a digital CDR with bang-bang phase detector and PI with discrete phases. We derive a set of compact formulas that include the effect of the phase noise of the oscillators (either free-running or PLL) and the finite number of phases of the PI on the output jitter. An eventdriven, behavioral simulator was developed to test our model. These formulas are validated over a wide parameter space and provide a useful tool to determine an initial estimation of the required number of phases of the PI, of the main parameters of the digital control algorithm, and to set limits to the phase-noise of the oscillators. Different strategies to elaborate the Early/Late (E/L) response of the Alexander algorithm on deserialized data are analyzed and compared. It is found that voting increases the output jitter due to the phase noise of the oscillators but keeps the jitter due to quantization of the PI under control, provided the loop delay is not so large.

1.2 DERIVATION AND VERIFICATION OF THE ANALYTICAL MODEL FOR JITTER

To derive the analytical formulas for the CDR jitter (difference between the timing of received data) we start from the linear model in Fig. 1(a), assuming a system with a single integrator (i.e., a first order CDR). The applicability of our model to second-order CDR will be discussed in Appendix C. As far as the phase noise of the oscillators is concerned, the linear model of Fig. 1(a) gives

$$\frac{\phi_{\mathrm{CDR}}}{\phi_{\mathrm{CK}}} = \frac{j\omega}{K + j\omega} = \frac{jf/\mathrm{BW}}{1 + jf/\mathrm{BW}} \qquad (1)$$

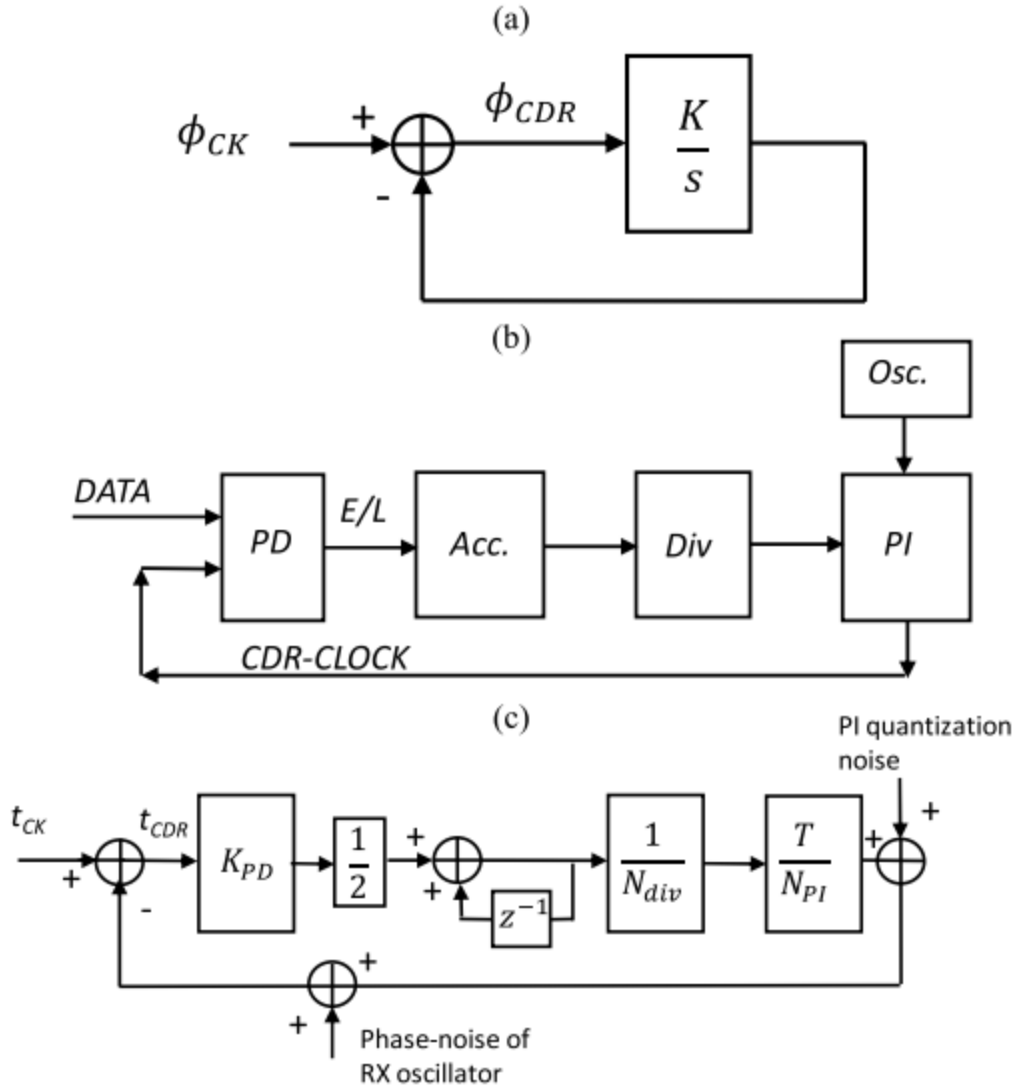

Fig. 1. (a) Linear model in the Laplace domain of a generic CDR with single integrator considering the phase of the transmitter clock as input. (b) CDR implementation considered in this article: after the phase detector we have an accumulator, a divider (i.e., the output of the accumulator is divided by a given factor discarding some of the least significant bits), and then the PI that generates the CDR clock from a local oscillator. (c) Linear model in the z-domain of the scheme in (b). tCK is the jitter of the transmitter clock, whose period jitter is indicated by σosc,p in the text for a free-running oscillator, while tCDR is the jitter of the reconstructed clock with respect to the timing of the received data. (c) Also indicates the other sources of jitter, i.e., the quantization of the PI phase (whose rms value is indicated as σquant in the text) and the noise of the RX oscillator (that in this model is indistinguishable from the one of the TX).

where the bandwidth is BW = K/(2π). The estimate of the K parameter depends on the system architecture. Fig. 1(b) considers the case where the E/L detection is performed directly on the serial data-stream, that will be analyzed in detail.

1.3 Free-Running Oscillator and E/L Detection on Serial Data

The simplest case concerns E/L detection on the serial stream, with transceiver and receiver clocks generated by freerunning oscillators. For simplicity, we consider only the noise of the transmitter free-running oscillator. Its phase noise power spectral density (PSD) as a function of the offset frequency f is given by

$$S_{\phi \mathrm{CK}\phi \mathrm{CK}} = \frac{A}{f^2} \qquad (2)$$

where we do not consider flicker noise to simplify the analysis and get close-form expressions. The inclusion of flicker noise would also require going to a second-order CDR. To determine the constant A, we note that the period jitter corresponding to (2) is [15]

$$\sigma^2_{\mathrm{osc},p} = \int_0^\infty \left|1 - z^{-1}\right|^2 \left(\frac{T}{2\pi}\right)^2 S_{\phi \mathrm{CK}\phi \mathrm{CK}} df \cong \frac{AT^3}{2}. \qquad (3)$$

We can thus write

$$S_{\phi \mathrm{CK}\phi \mathrm{CK}} = \frac{2\sigma^2_{\mathrm{osc},p}}{T^3 f^2}. \qquad (4)$$

Working with time is easier than using phases: we consider the block diagram of Fig. 1(c) corresponding to the architecture in Fig. 1(b). If we assume for the transmitter oscillator the phase noise spectrum of (4), the rms value of the absolute jitter of the recovered clock compared to the received signal [i.e., the rms value of the variable t CDR in Fig. 1(c)] due to the noise of the oscillator only is

$$\sigma^2_{rj} = \frac{T^2}{4\pi^2} \int_0^\infty \frac{2\sigma^2_{osc,p}}{T^3 f^2} \frac{f^2/\mathrm{BW}^2}{1 + f^2/\mathrm{BW}^2} df = \frac{\sigma^2_{\mathrm{osc},p}}{4\pi T \mathrm{BW}}. \qquad (5)$$

Notice that (5) links the absolute jitter of the CDR to the period jitter of the transmitter clock. In Fig. 1(a), consistently with the event-driven simulations, the jitter is applied to the transmitter clock. However, the jitter of the oscillator in the receiver has exactly the same effect [see where

the noise of the RX oscillator is added in Fig. 1(c)], so that σ2 osc,p in (5) is indeed the sum of the square of the period jitter of both transmitter and receiver oscillators.

To compute the CDR bandwidth, although the model of the accumulator is in the z-domain, since the CDR bandwidth is much smaller than the data rate, we can approximate it as

$$\frac{1}{1-z^{-1}} = \frac{1}{1-e^{-sT}} \sim \frac{1}{sT}. \qquad (6)$$

The block 1/2 in Fig. 1(c) comes from the consideration that, on average, we have 0→1 and 1→0 transitions only in half of the bit periods. Comparing Fig. 1(a) and (c) and using (6) we get

$$K = K_{\mathrm{PD}} \frac{1}{2N_{\mathrm{div}} N_{\mathrm{PI}}}. \qquad (7)$$

That implies

$$\mathrm{BW} = \frac{K}{2\pi} = K_{\mathrm{PD}} \frac{1}{4\pi N_{\mathrm{div}} N_{\mathrm{PI}}}. \qquad (8)$$

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II.EXISTING SYSTEM AND PROPOSED SYSTEM

2.1 EXSISTING METHOD

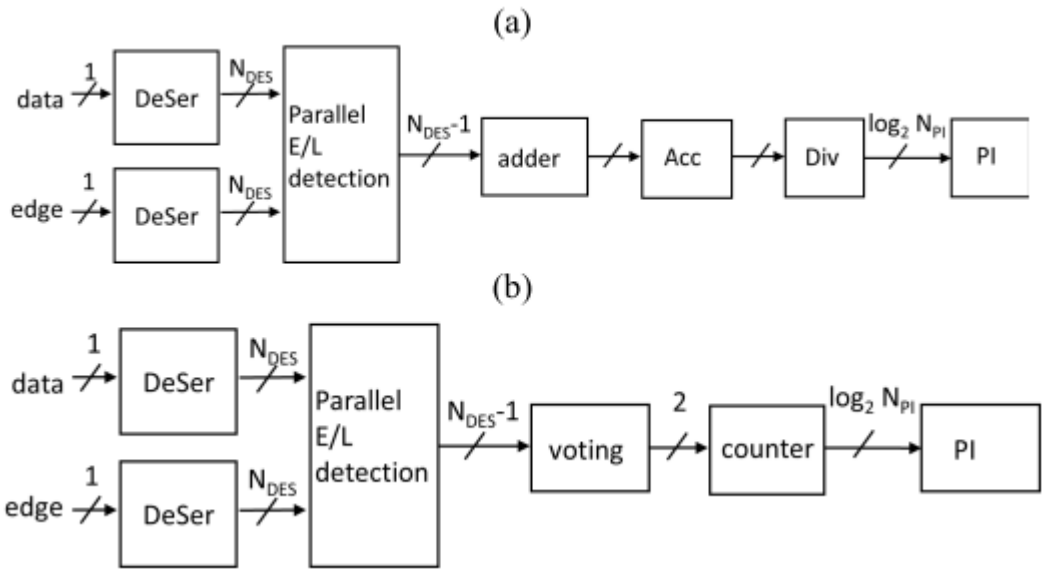

FiG2.1. Example of CDR algorithms performing the E/L detection on deserialized data and edge samples.

In both cases, the PI code is updated after NDES data periods. (a) E/L resulting from the parallel data are summed together (with sign) and then accumulated and divided before driving the PI. The voting in (b), instead, produces "up" and "down" signals for the counter that drives the PI.

2.2 PROPOSED METHOD

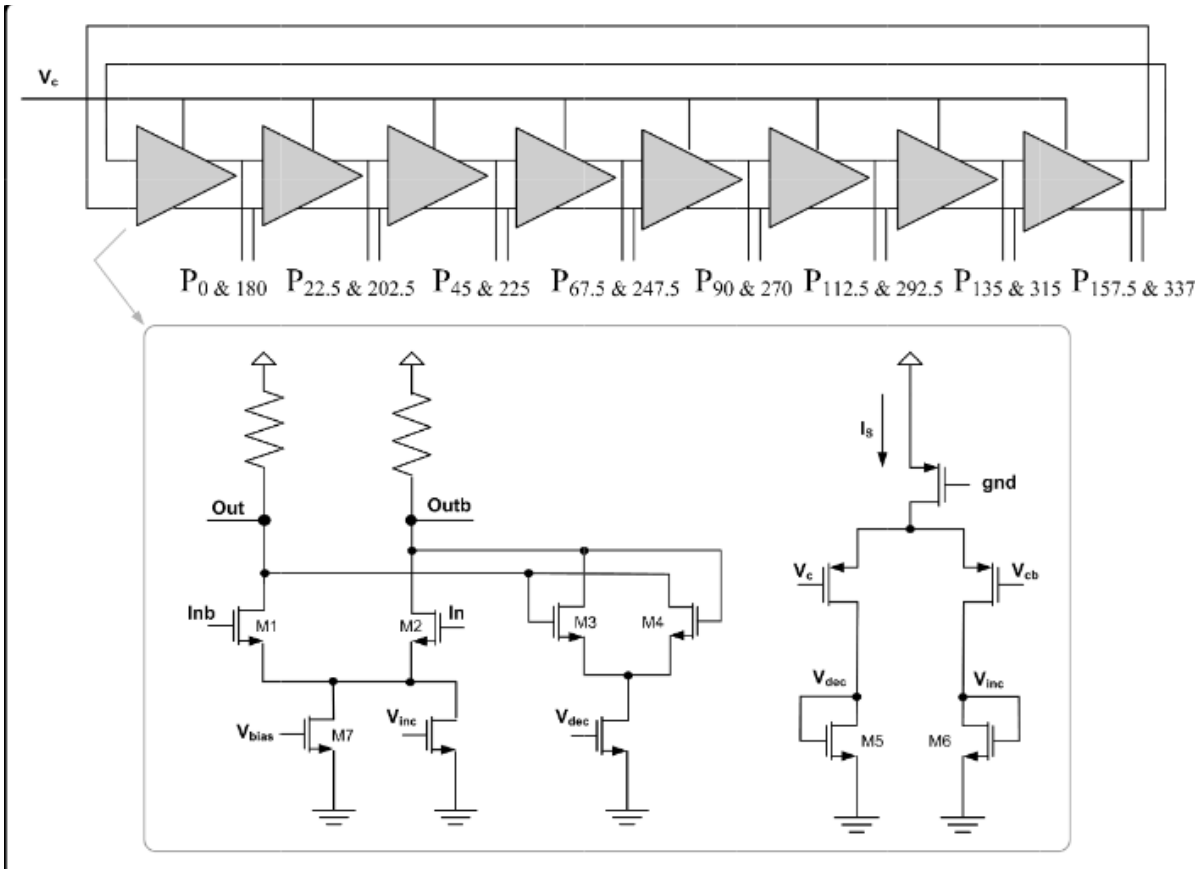

Fig2.Cdr-Pll Eight Stage Voltage Controlled Ring Jitter Oscillator

The results of design and transistor level simulation of a novel architecture for PLL-based clock and data recovery (CDR) circuit are presented in this chapter. The proposed PLL-based CDR is a referenceless quarter-rate design (i.e., the clock frequency is quarter the input data rate), comprising a novel quarter-rate phase detector, a novel quarter-rate frequency detector and can be used in a deserializer as part of the Serializer/Deserializer (SerDes) device usually utilized in inter-chip communication networks [34]. The proposed CDR circuit is designed in a standard LT-SPICE CMOS technology, and simulated at transistor level to verify its accuracy as well as to evaluate its characteristics and performances.

Voltage Controlled Oscillator of For proper operation of the phase and frequency detectors, eight clock signals and their complements (separated by 22.5º) are required. Due to its wide tuning range an eight-stage ring oscillator structure was chosen. As shown in Figure 2, the VCO consists of eight stages, each one of them comprising a delay cell and a control circuit for generating differential control voltages Vinc and Vdec for the delay cell. The controlling signals Vinc and Vdec can be viewed as differential control lines and hence providing higher noise immunity to the VCO controlled input. The dimensions of transistor M7 and the voltage at its gate Vbias should be carefully adjusted such that proper VCO gain, linearity and tuning range will be obtained and based on the concept of bias current controlled negative resistance . As the bias current of the cross-coupled pair of transistors (M3 and M4) increases, their negative small-signal resistance becomes less negative; hence the total resistance seen by the outputs nodes out and outb increase, thereby lowering the oscillation frequency.

Clock and Data Recovery (CDR) is a critical component in communication systems, especially in high-speed serial data transmission. The purpose of CDR is to recover a stable clock signal and extract data from the incoming serial bitstream. The algorithm for CDR varies depending on the specific requirements of the system, the characteristics of the transmitted data, and the technology used. Here, I'll outline a basic concept of a CDR algorithm.

Basic CDR Algorithm:Phase-Locked Loop (PLL):

Many CDR algorithms use a Phase-Locked Loop (PLL) as a fundamental building block. The PLL aims to generate a stable clock signal synchronized with the incoming data.

Phase Detector:

The phase detector compares the phase of the recovered clock signal with the incoming data. It generates an error signal based on the phase difference.

Loop Filter:

The error signal is filtered through a loop filter to smooth out fluctuations and noise. The filtered signal is used to control the frequency and phase of the voltage-controlled oscillator (VCO) in the PLL.

Voltage-Controlled Oscillator (VCO):

The VCO generates the recovered clock signal. The frequency and phase of the VCO are adjusted based on the filtered error signal from the loop filter.

Frequency Divider (optional):

In some CDR implementations, a frequency divider may be used to obtain a lower-frequency clock output while maintaining synchronization.

Data Detection:

In addition to clock recovery, the CDR algorithm often includes a data detection mechanism. This involves sampling the incoming data at the recovered clock edges to correctly interpret the transmitted bits.

Data Sampling:

The incoming data is sampled at the edges of the recovered clock signal.

Decision Feedback:

Decision feedback techniques may be employed to make decisions about the sampled data. This involves comparing the sampled data to decision points and adjusting the decision thresholds based on past decisions.

Bit Synchronization:

The combination of clock recovery and data detection ensures proper bit synchronization, allowing accurate recovery of the transmitted data.

Advanced Techniques:

In advanced CDR implementations, additional techniques may be used, such as:

Adaptive Filtering: Dynamically adjusting filter parameters based on the characteristics of the incoming signal.

Phase Interpolator: Interpolating the phase between clock edges for more accurate clock recovery.

IV. RESULTS AND ANALYSIS DISCUSSION

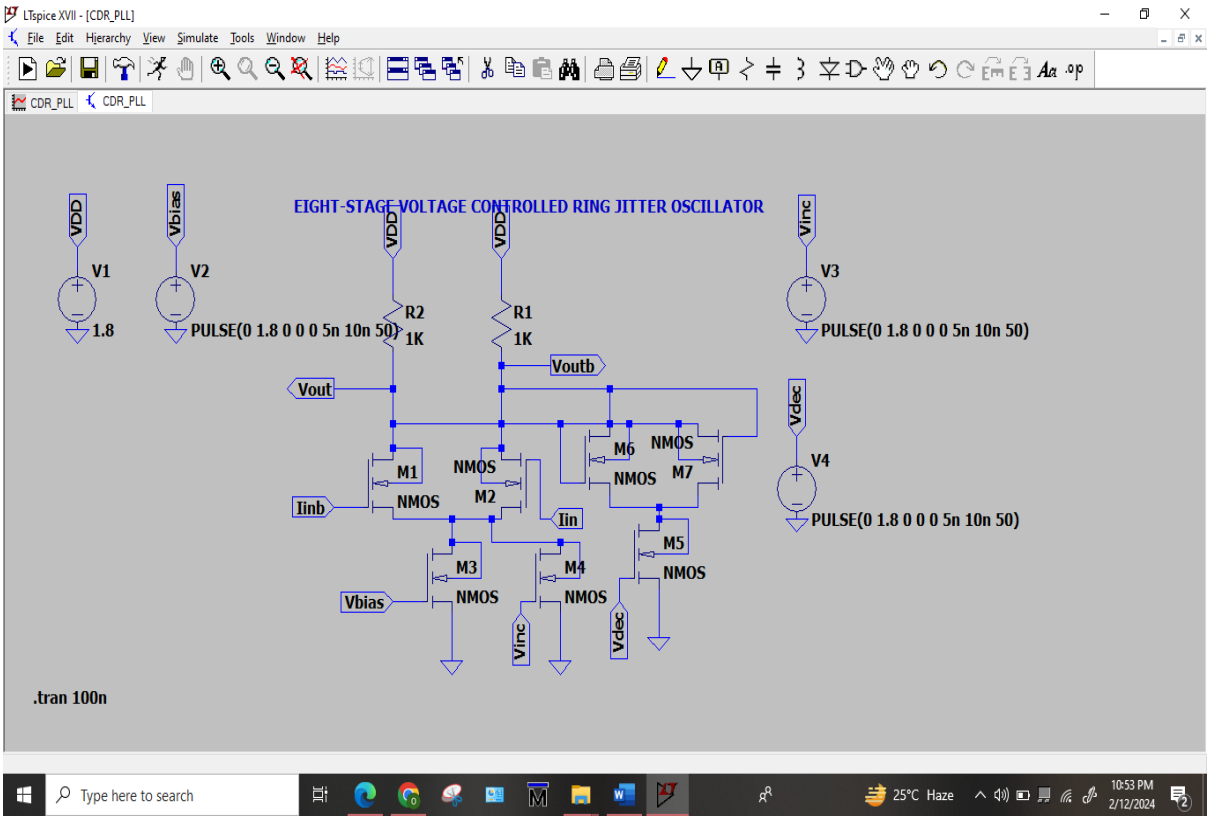

Fig.1.CDR-PLL multi stage(8) circuit

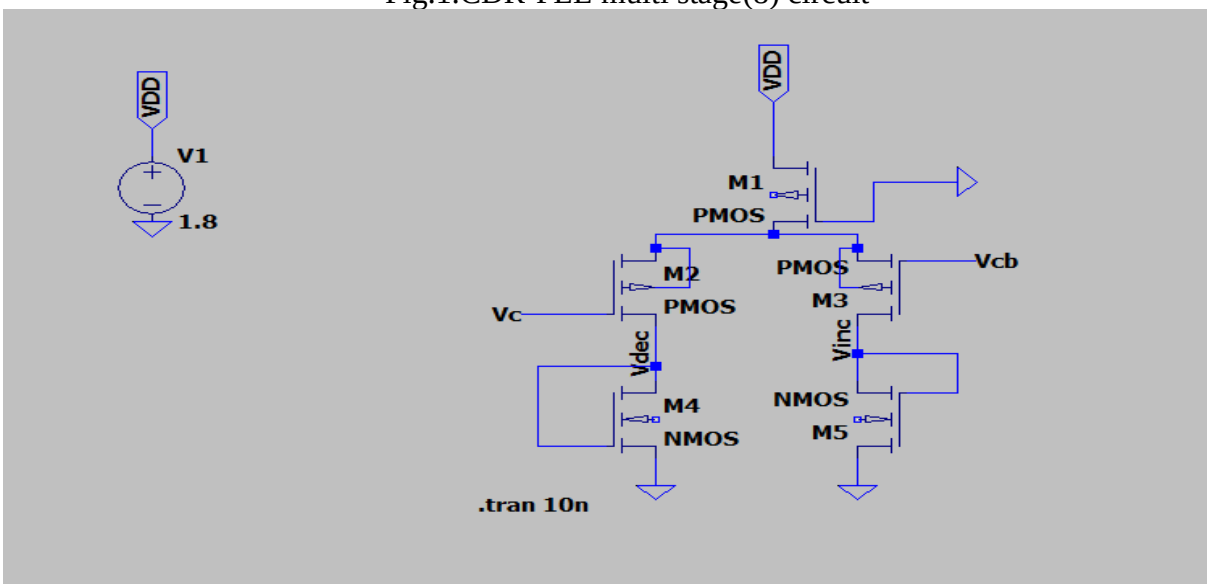

Fig.2.CDR-PLL single stage circuit

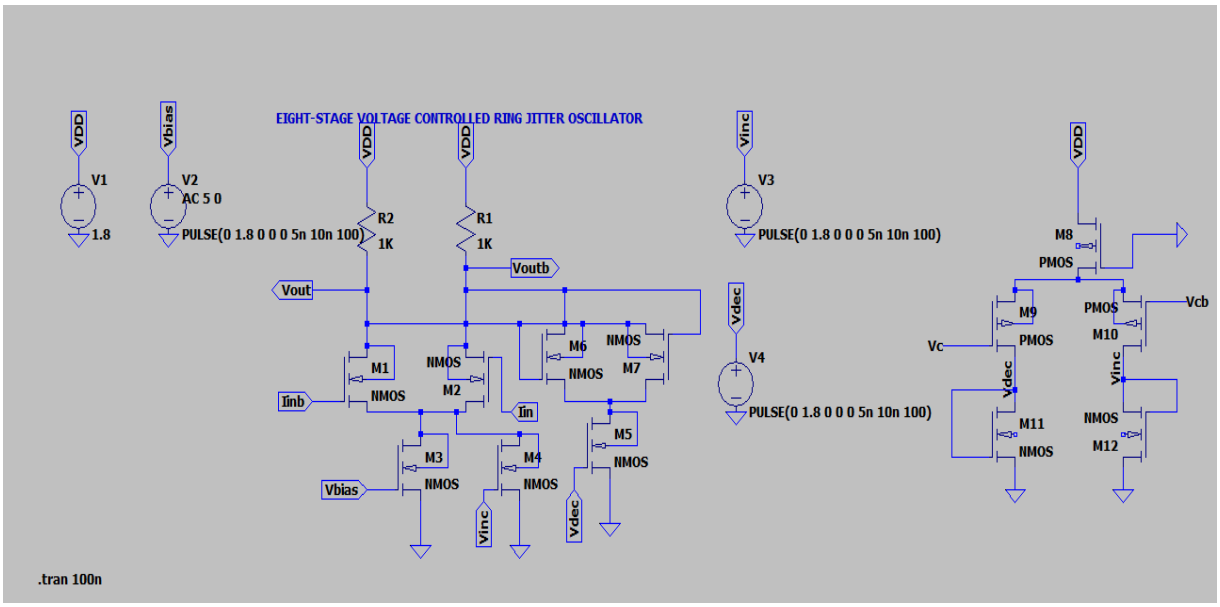

Fig3.combination of both single and multi-stage circuit

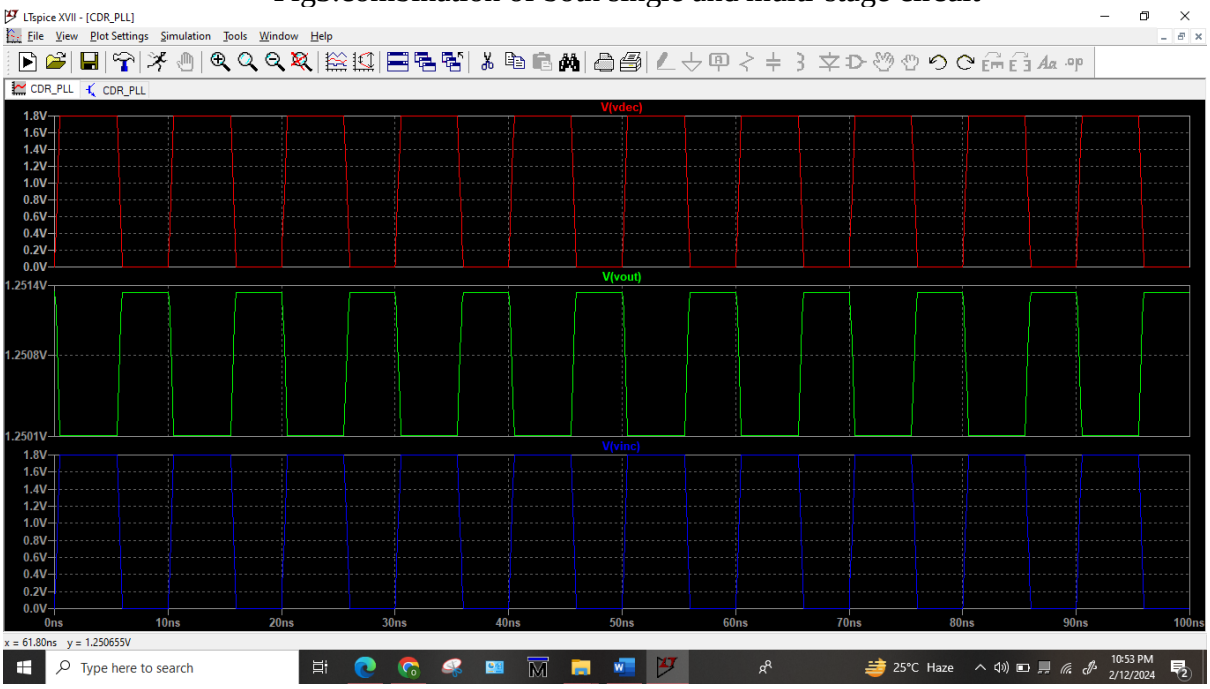

Fig4 output waveform of CDR PLL multi-stage circuit.

CONCLUSION

We have derived a set of simple for a first order estimate of the CDR jitter due to noisy oscillators as well as quantization of the PI phases including also effects such as voting and loop latency. These formulas match quite well the event-driven behavioral simulations on LT Spice. The latter requires in any case less than a minute to perform a simulation, so that the main

advantage of the compact formulas is to show the main tradeoff and guide in the initial phases of the design. The analysis identifies a tradeoff in the choice of the number of PI phases: few phases result in higher quantization jitter, whereas a large number of phases reduces the CDR bandwidth.. The analysis presented here assumed an ideal channel without intersymbol interference and noise. Inclusion of a realistic channel response into the model is ongoing. In conclusion, the future of CDR (Clock and Data Recovery) and PLL (Phase-Locked Loop) algorithms is poised for significant advancements driven by the increasing demand for high-speed and reliable data communication across various applications. The convergence of technological innovations, such as higher data rates, adaptability to variable conditions, low power consumption, and advanced signal processing techniques, will shape the trajectory of these algorithms.

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