MIXING DRIVERS IN CLOCK-TREE FOR POWER SUPPLY NOISE REDUCTION

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ABSTRACT

In today's process technologies, power supply noise may cause serious clock jitter and circuit malfunction. Noise occurs by the fast and simultaneous voltage switching. A primary contributor to the noise is the clock-tree and the underlying sequential circuits that switch simultaneously, thus causing high current peaks. This work proposes to spread the switching of the clock-tree drivers, while maintaining low skew at the sinks of the tree, where the clocked circuits are connected. Driver switching characterization has been used for fast computation of peak currents, delays and slopes, integrated in a two phase algorithms. It first constructs the clock-tree in a top-down traversal, employing a mix of high threshold voltage (HVT) and weak low threshold voltage (LVT) clock-drivers. A bottom-up delay correction phase then takes place, aiming at clock skew minimization. The algorithm was implemented in 40 nano meters TSMC process technology, achieving 35% to 70% clock-tree peak current reduction, translated to similar reduction in power supply noise. The proposed method can easily be combined with other existing methods to further reduce the noise.

KEYWORD--CLOCK DRIVERS, CLOCK NETWORK, CLOCK-TREE, POWER SUPPLY NOISE.

1.INTRODUCTION

The power supply instantaneous voltage drop in today's VLSI designs, known as power supply noise (hence forth noise for short), is a major concern. Noise of a very few hundreds milli volts causes clock jitter and circuit malfunction. Process technology scaling escalates the fluctuations occurring in VDD and VGND. There, the underlying resistance, capacitance and peak current switching DI/DT are growing up, thus increasing the noise. Power noise analysis comes to the simple ohm law of multiplying peak current by the power network impedance and high capacitance has been extensively studied. We focus on reducing the peak current I and its time derivative DI/DT, which has also been treated by various techniques. Peak current reduction achieves the following goals:

1) Reduction of the on-die IR voltage drop, where the resistance dominates the impedance.
2) Reduction of the L(DI/DT) voltage drop occurring at the package level, where the inductance dominate the impedance.
3) Reduction of the clock jitter which is directly affected by IR voltage drop.
4) Improving the utilization of the de-coupling capacitors by increasing their effective distance that is inversely proportional to DI/DT.

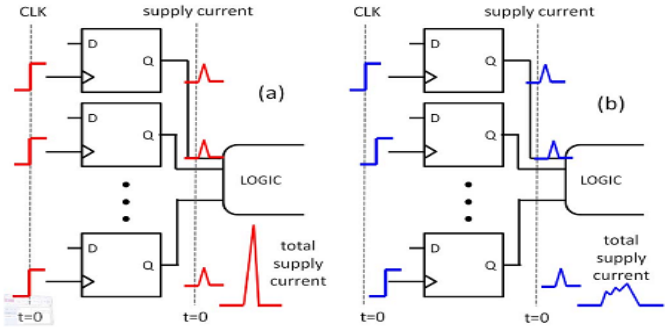


Fig1. Peak supply current reduction by clock signal misalignment

The clock related voltage switching is a primary contributor of the power noise, while the logic signal switching is spread over the entire clock cycle. The switching of the clock tree and the sequential circuits is occurring simultaneously, causing high current instantaneous peaks. The clock network is therefore a natural candidate to treat for peak current remedy. To obtain proper and robust sequencing of the logic, the clock skew must stay within prescribed limits, usually not exceeding 5% of the clock cycle. Peak current reduction is therefore a delicate task, for which several approaches have been proposed. Peak current reduction by minimizing its component caused by the flip-flops (FF's) switching was first proposed. Its underlying idea is illustrated in fig1. A clock rescheduling procedure was proposed which utilized the allowable skew. Skew consumption technique was first presented in for timing optimization. Claims for 30% reduction of the peak current drawn by the clock network, without sacrificing the clock frequency. A refinement of presented in which accounted the switching of deeper logic levels. Peak current reduction of 12% was claimed yielding 19% reduction of the power supply voltage variations. The work presents another technique of dividing the allowable skew time intervals into slots. The clock timing of each FF was then allowed to some slot in an attempt to reduce the peak current. 17% peak current reduction was claimed. There is a problem in skew spreading though, clock rescheduling for purposes other than timing convergence may considerably complicate the underlying design and techniques as time-borrowing may not be applicable.

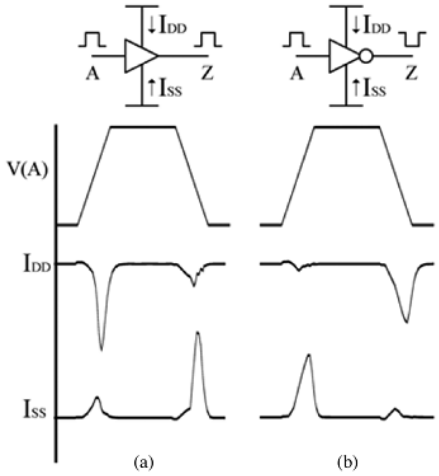


Fig2 .The idea of buffer polarity assignment.

In (a), the buffer exhibits high current at the rising edge of the clock signal. In (b), an opposite situation occurs for an inverter.

A problem arising by the clock-driver polarity method is the uncontrolled skew occurring by different delays of inverters and buffers residing along root-to-sink clock paths. Clock skew aware polarity assignment was also proposed in which still used single size clock-drivers. A solution of noise reduction combining sizing and polarity was described in it. It was lately enhanced to support multiple power modes by dynamically controlling the internal delay of the clock-drivers.

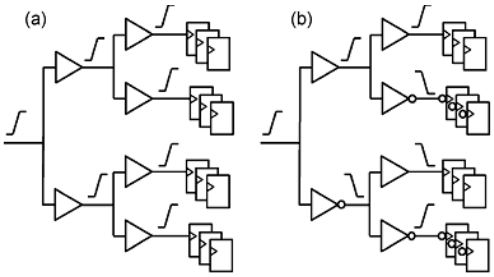


Fig3. Mixing polarities of clock-drivers and FFs

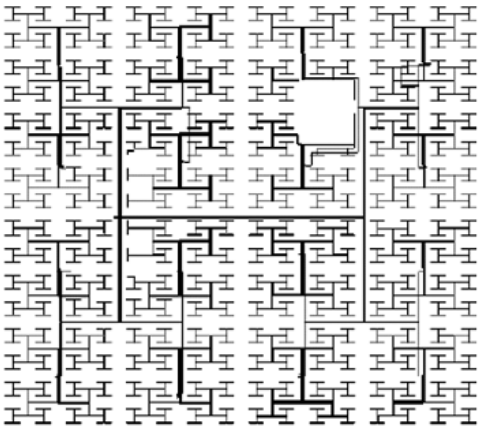


Fig4. An H-tree network used by IBM\ MOTOROLA power pc processor.

2. EXISTING SYSTEM:

We subsequently present an algorithm to reduce the peak current and maintain minimum skew, by the tree modifications and wire lengths adjustments illustrated in the algorithm. The algorithm comprise two phases, the first is a top-down traversal. It's primary goal is to cut the peak supply current. It also maintains small skew in an ad-hoc manner, ensuring it does not escape at the tree's leaves. That is a good starting point to a second phase of bottom-up traversal, aiming at skew mollifying by fine adjustments of the clock-drivers positions in the tree branches. The second phase has a very small impact on the peak current, which has already been reduced in the first phase.

Starting at the root, for each visited node, the top-down traversal does the following:

1. substitution of a fork mixing HVT and LVT/2 drivers as illustrated in fig.
2. For both the HVT and LVT/2 fork's branches, the cumulative from the root and the slope at the branch driver's output are calculated.
3. The position of the HVT driver's is adjusted to ensure equal delay from the root to the far end HVT and LVT/2 drivers. Delay equalization is done by numerical binary search iterations using the driver's characteristics presented in the section.

Micro wind is a tool for designing and simulating circuits at layout level. The tool features full editing facilities various views (MOS characteristics, 2D cross section, 3D process viewer), and an ANALOG simulator. DSCH is software for logic design. Based on primitives, a hierarchical circuit can be built and simulated. It also includes delay and power consumption evaluation. Silicon is for 3D display of the atomic structure of silicon, with emphasis on the silicon lattice, the dopant and the silicon dioxide. It is truly integrated EDA software encompassing IC designs from concept to design beyond their imagination. Micro wind integrates traditionally separated front-end and back –end chip design into an integrated flow, accelerating the design cycle and reduced design complexities.

DISADVANTAGES OF EXISTING S/M:

1. Power consumptions are carried out without any noise disturbances.
2. Not accurate due to simple controller.
3. Network management can be hard enough for the dealers.
4. Need expert people on the driver maintenance systems.
5. Active logs are on the driver characteristics.

3. PROPOSED SYSTEM:

In this system improved built-in extractor which generates a spice net list from the schematic diagram. It generates a VERILOG description of the schematic for layout conversion. Immediate access to symbol properties(Delay, fan out). Model assembly support for 8051 and PIC 16F84 microcontrollers. Sub-micron, deep-submicron, nano-scale technology support and supported by huge symbol library.

PRO THUMB (Mix-signal simulator):

No spice or external simulator is needed for verification of CMOS circuits. Micro wind program has in built ANALOG like simulator which supports MOS level 1, level 3 or BSIM4 model. With features like fast time-domain, voltage and current estimation, very intuitive post processing, frequency estimation, delay estimation, makes PRO thumb a time saver. Even power estimation of circuit simulation can be checked on-screen.

It has some important points are:

1. Built-in spice like ANALOG simulator.

2. Features fast time-domain, voltage and current estimation with very intuitive post processing: frequency estimation, delay estimation.

3. It supports level1, level3 and BSIM4 models for all technologies from 1.2um till 22 nm.

4. MOS characteristic viewer with access to parameters of main model. Time domain voltage and current waveforms are available at the press of one single button.

5. Time domain voltage and current waveforms available at the press of one single button.

6. DC/AC characteristics signal frequency vs time , eye diagrams MIN/TYPE/MAX ANALOG simulation.

PROTUTOR (MOS Characteristics tutor):

Valuable screen to understand the MOS characteristics, with a user interface that designers will like. Change the model parameters and see their effects on ID/VD, ID/VgId(log)/vg, threshold vs length. You can also fit the simulations with measurements we made in test-chips fabricated in 0.35, 0.25 and 0.18um. in the manual, a tutorial on MOS models is given, with details on all parameters.

MEMSIM (Floating gate memory simulator):

The double-gate MOS has been introduced in MICRO WIND for the simulation of non-volatile memories such as EPROM, EEPROM and FLASH. The command UV exposure erases floating gates and removes all electrons. The programming is performed by a high voltage supply on the gate (7V in 0.12um).

MICRO WIND TOOL DESIGN FLOW:

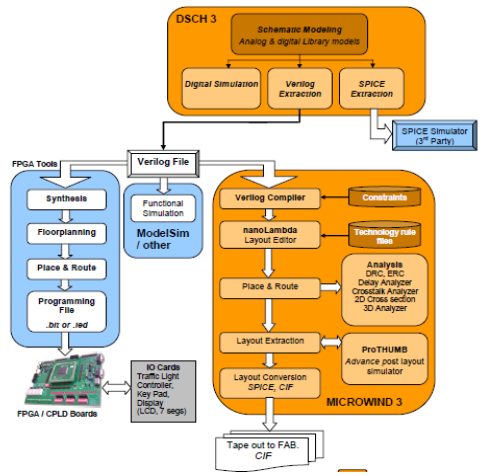


Fig5. Circuit design flow diagram

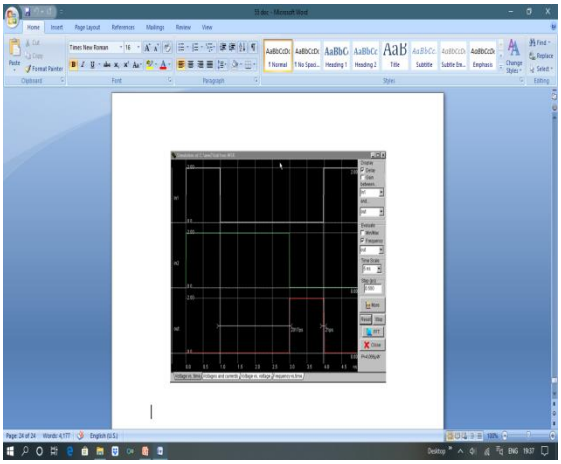
Integrated circuits have changed the way of our life. Your name one gadget and will find the power of silicon which has made such complex electronic circuit possible. Integrated circuits come in many different flavours these days. User designed chips in CPLDs and FPGAs have revolutionized the way of system design. But ASIC remain in lead due to their speed, power

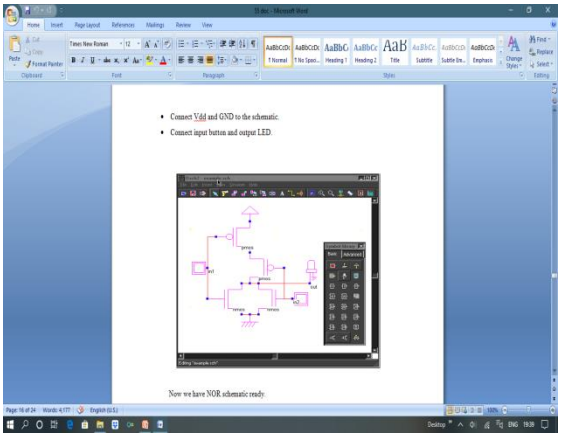
and performance advantages. Every critical system design is flagged with ASICs. To learn the IC design process, techniques & critical requirement handling is required.

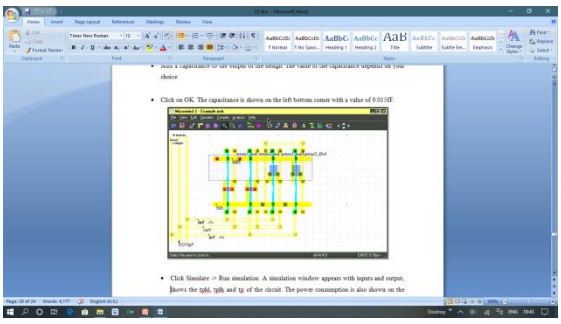
ADVANTAGES OF PROPOSED S/M:

1. Noise reduction is more efficient when compared with the previous details.
2. No time delay and interferences.
3. Power variations are less with respect to the proposed ones.

RESULTS:







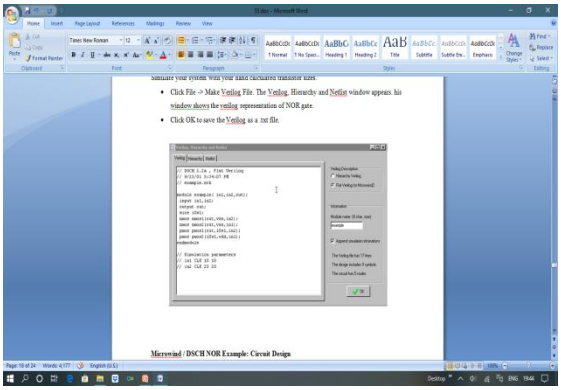


Fig6. Screenshots of the simulations in the mixing drivers and clock tree.

Hence the final results of the simulations shows that the power variations can be decreased from the higher range values to the lower range values.

5 .CONCLUSION & FUTURE SCOPE:

We are proposed to reduce the peak supply current and its time derivative by spreading over time, the switching of the clock-tree drivers, while maintaining low skew at the sinks of the tree. Although the objective of the study was achieved, there were a few limitations in the project which can be evaluated based on the driver techniques. The future variations can reduce the total power wastage by increasing the clock speed or any other method.

REFERENCES:

1. M. popovich, A. V. Mezhiba and E.G.Friedman, power distribution networks with on-chip decoupling capacitors, New York- springer, 2008, vol. 13.
2. R. Joseph, D. Brooks, and M. Matonosi, “control techniques to eliminate voltage emergencies in high performance processors,” in proc. 9th IEEE Int. symp. High-perform. Comput. Archit. (HPCA-92003), PP. 79-90.
3. M.S. Gupta, J.L. Oatley, R. Joseph, G-Y. Wei, and D.M.Brooks, “understanding voltage variations in chip multiprocessors using a distributed power-delivery network”, in proc. IEEE design , autom test EUr. Conf. Exhib, pp 1-6.
4. L.D. Smith, R.E. Anderson and T. ROY, “chip-package resonance in core power supply structures for a high power micro processors, in proc.ASME Int. Electron package. Tech conf. Exhib, Kausai, HI, USA, 2001, P.5.
5. N.H.E. WESTE AND D.M.HARRIS, Integrated circuit design, upper saddle river, NJ,USA: Pearson,2011, ch.12.
6. E.SALMAN AND E.FRIEDMAN, high performance integrated circuit design, New York: McGraw Hill professional, 2012, ch. 10.

7. L-T. Wang, Y-W- CHANG and K.T. Tim chang Electronic design Automaton: synthesis, verification, test. S an Francisco, CA, USA, Morgan Kaufmann, 2009, ch.113.

8. Y.KIM, S.HAN , and J.KIM, " POWER SUPPLY NOISE REDUCTION BY CLOCKSCHEDULING WITH GATE-LEVEL ; Soc design of vol2

9. T. Xanthopoulos, Clocking in modern vlsi systems, new York: springer, 2009, ch.2.

10. J.P. Fishburn, "clock skew optimization", IEEE.