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# POWER OPTIMIZED 8 BIT MULTIPLIER DESIGN USING GDI TECHNIQUE

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## Abstract

The multiplier finds usage in many kinds of processing systems ranging from application specific processors to small scale general processors. This paper presents the implementation of a low power and area 8-bit multiplier using full adder cell based on Gate diffusion input (GDI) technique. The tool used for the simulation of the circuits is Tanner EDA 13.0 and the simulation is done using T-spice. The most vital requirement of any processor would be speed, area and power. As in this paper the multiplier is designed using GDI technique, it helps to reduce the area constraints of the design with their minimal implementation logic. Therefore the design proposed in this project would give a circuit which have high speed, high area efficiency, reduction in delay and also it consumes less power.

## 1 Introduction

An increase in the level of integration in modern Very Large Scale Integration (VLSI) technology has rendered possible integration of many complex components in a single chip. Moreover, an analog circuit techniques in the front end wireless communication demand for a digital domain to save power. In most of these applications, multipliers have been an obligatory component and determine overall circuit performance with respect to speed, power consumption and size. Hence, the goal of this project is formulated to design a multiplier with less delay, low power consumption and compact area. In general, the performance of multiplier in terms of delay, power consumption and area can be improved by two methods. First one is based on efficient implementation of multiplier function, whereas, another relies on proper selection of logic style for its implementation. There have been various multiplication methods for realizing the low power and high speed multiplier introduced in the last few decades. However, in these multiplication techniques, the intermediate computation involved in the multiplier operation reduces the speed exponentially in accordance with the width of the multiplier input bit. This becomes a critical issue for a higher number of input bits .But this issue can be mitigated by using the Gate Diffusion Input (GDI) Technique.

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As stated earlier, the logic styles used for realizing the multipliers have significant influence on the speed, size, power consumption and wiring complexity. Numerous logic styles in the classes of static Complementary Metal Oxide Semiconductor (CMOS), dynamic, transmission gate, Pass Transistor Logic (PTL) and Gate Diffusion Input (GDI) logic are discussed in the literature. Among them, GDI is considered in this project implementation due to its merits of low power consumption and implementation of any functions with low transistor count. However, the gates based on this logic are suffered from a low output voltage due to the threshold voltage drop. This has motivated us to propose an improved set of gates that operate with merits of full swing without increasing the fabrication complexity with the possibility of implementing with less transistor count.

A multiplier is considered as an area consuming element and also its performance determines the performance of the whole system, hence it is necessary to design a multiplier which requires less area and consume low power. A normal CMOS multiplier actually occupies a substantial power and greater amount of area, hence there is a need to further reduce the number of transistors while designing the multiplier. And this can be implemented by using a revised CMOS logic which is called as Gate Diffusion Input (GDI) technique . Actually this method permits the execution of bulk of complicated logic functions by using only two transistors. The main objective of the project is to design the low power and high-speed multiplier using the Gate Diffusion Input (GDI) technique, which reduces the area, delay and power consumption, in addition it also achieves the high performance. And finally, the GDI technique is compared with the other technique of multiplier design like CMOS technique.

In this proposed methodology, the multiplier is designed using the Gate Diffusion Input (GDI) technique. It is a new technique of low power digital circuit design. This GDI technique allows reducing power consumption ,delay and area of digital circuits besides maintaining the low complexity of logic design .Main advantage of using GDI technique while designing the multipliers is a complex logic functions can be easily implemented just by using two transistors .So by using this technique we can reduce the transistor count. It can be seen that large number of functions can be implemented using the basic GDI cell. For instance, MUX design is the most complex design that can be implemented with GDI, which requires only 2 transistors, which requires 8-12 transistors with the traditional CMOS or PTL design. Many functions can be implemented efficiently by GDI by means of transistor count. However, to implement NAND, NOR it requires 4 transistors as that in Static CMOS design. NAND and NOR the

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universal logic gates, any Boolean Function can be implemented using these gates, are most very efficient and popular with static design style. Function1 and Function2 are universal set for GDI, and consists of only two transistors, compared to NAND and NOR. These functions can be used synthesize other functions more effectively than NAND and NOR gates.

So by using this Gate Diffusion Input (GDI) technique, the design of AND gate and Full Adders is implemented which are the main building blocks of the Multiplier design.

As the design of the multiplier is performed using the Gate Diffusion Input (GDI) technique which is the advanced digital circuit designing technique, it offers reduced area, less power consumption, high speed when compared with the CMOS technique. Another important significance of the Multiplier design using GDI technique is, it provides the circuit with reduced number of transistors.

## 2 Literature Survey

An extensive literature survey is carried out in order to confirm the need for the proposed objective. Initially, the reason for selection of GDI logic and its bottlenecks are explained, and then the full swing mechanisms available in the literature for GDI logic are discussed

### Complementary Pass Transistor Logic

The Complementary pass-transistor logic (CPL) full adder having 32 transistors and using the CPL gates has been designed. The complexity of full CMOS pas gate logic can be reduced dramatically by adopting another circuit called CPL. The main idea behind CPL is to use a purely NMOS pas transistor network for the logic operations. All the inputs are applied in complementary form. i.e.: every input signal and its inverse must be provided. The circuit also produces complimentary output, to be used by subsequent CPL

**Israel A.Wagner et al**. has examined the Gate Diffusion Input (GDI) approach for the reduction of power consumption in logic circuit design. The prevalence of this design technique over standard CMOS logic style and PTL (pass transistor logic) with glance to power dissipation, area multiplicity and propagation delay has also described A new approach of digital circuit design with low power has examined. This approach helps in decreasing the propagation delay, area and power consumption which also maintains the low complexity of the circuits. In this paper, operation illustration with standard CMOS process and pass-transistor logic (PTL) design techniques have been described. The different processes have distinguished in terms of area, number of transistors, propagation delay, and power dissipation. The advantages and disadvantages of Gate diffusion input technique compared to other process has also been examined. Numerous logic circuits have been actualized in different design methods.

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**M. Mohanapriya et al**. has examined the delay, area and power dissipation analysis of adder topographies [2]. This paper presented the appropriate option for the selection of the adder topology related with the parameters like power dissipation, delay and area. This paper has evaluated the operational and performance parameters like area, power dissipation and propagation delay. In this research work, the functions of adders were analyzed for the optimization of power dissipation, delay and area. These adders have been generally used in several applications such as in digital system, control system and digital signal processing.

## 3 Proposed Methodology

### Gate Diffusion Input

Gate diffusion input is a novel technique for low power digital circuit design in an embedded system. This technique allows reduction in power consumption, delay and area of the circuit. This technique can be used to reduce the number of transistors compared to conventional CMOS design. Recently, a novel design called Gate-Diffusion Input (GDI) is proposed by Morgenshtein et. al.. It is a genius design which is very flexible for digital circuits. Besides, it is also power efficient without huge amount of transistor count.

The GDI scheme depends on the implementation of an elementary cell as Principally, this GDI cell looks like a CMOS inverter. However, there are a number of dissimilarities. The GDI cell involves three inputs:

1.) Standard gate input of PMOS and NMOS.

2.) P input to the source/drain of PMOS and

3.) N input to the source/drain of NMOS where bulk of PMOS and NMOS are associated to P or N.

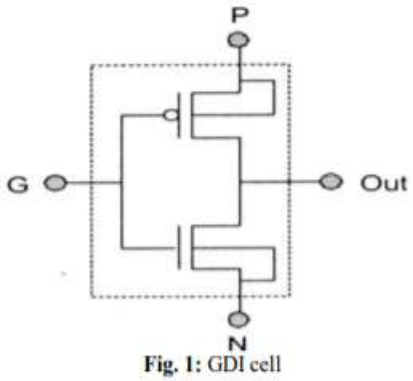

Fig. 1: GDI cell

It is observed that all of the functional operations are not possible in standard CMOS process but they can be strongly actualized in silicon on insulator (SOI) or CMOS technologies

| N | P | G | Out | Function |
|---|---|---|---|---|
| '0' | b | a | a'b | f1 |
| b | '1' | a | a'+b | f2 |
| '1' | b | a | a+b | OR |
| 'b' | '0' | a | ab | AND |
| 'c' | B | a | a'b+ac | MUX |
| '0' | '1' | a | a' | NOT |

**Table1 Various Logic Functions**

Table 1 represents that a small variation in the input line of the elementary GDI cell consistent to different Boolean functions. Generally, these functions are versatile in CMOS as well as in PTL implementations. But these functions are

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very simple in GDI design method. The GDI method is different from the other design techniques, and it has some valuable characteristics, that allow up gradation in design multiplicity level, power dissipation, and transistor count. Understanding of GDI cell needs a wide functional determination of the elementary cell in several cases and configuration. Firstly, we have designed the basic digital gates using GDI technique and then these gates are further used in the implementation of different types of adders and multipliers.

A full adder is implemented with the help of GDI technique. Here two GDI AND gates ,an XNOR and an XOR gate operate together to form the full adder. It is observed that GDI adder is the optimum adder based on power consumed. Hence the multiplier is implemented with the GDI Full adder.

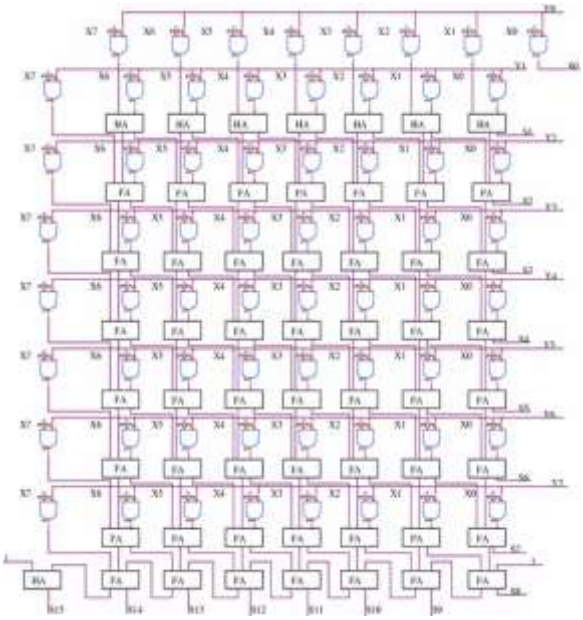

**Fig 1 Implementation Diagram of 8-bit multiplier**

The main important blocks of the 8-bit Multiplier that is going to be implemented using Gate Diffusion Input (GDI) Technique is the Full Adder which is designed using the GDI technique.

**Full Adder**

Full adder is a fundamental block in arithmetic and logic units which is a nucleus to perform various operations such as subtraction, multiplication, division and address computation as well as additions. Full adders are encountered in the critical path of the complex arithmetic computation like multiplication. Obtaining high operation speed at low power consumption is desirable which make the design of an adder very challenging. There are standard implementations from various logic styles that have been used in the past to design full adder circuit. These are varied in the way of producing intermediate nodes and outputs and transistor count. On one hand, a full adder design in static CMOS with pull up PMOS and pull down NMOS is the conventional design but it requires 28 transistors count Weste et al (2003). On the other hand, dynamic circuits can significantly reduce the transistor count but the incurred power consumption is high.

There are various full adders' designs discussed in the literature (Shams et al 2002; Hung Ten

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Bui et al 2002; Jin Fa Lin et al 2012 and Ramanamurty et al 2012). The full adder design discussed by Shams et al (2002) uses sixteen transistors and can provide the full swing output. Also, an improved ten transistors full adder design is discussed by Hung Ten Bui et al (2002), but it is suffered by threshold voltage problem. To overcome this issue, buffering circuit based PTL full adder is introduced by Jin Fa Lin et al (2012). A MUX based Shannon full adder using fourteen transistors is discussed by Ramanamurty et al (2012). Though the design is superior in energy consumption, this scheme suffers from a setback of low driving capability.

From all these the final inferred conclusion is that, the design for high speed, low power consumption full adder can be achieved only by reducing number of transistors while designing the full adder. This can be achieved using Gate Diffusion Input Technique

**Design of Gates using GDI Logic**

The gates required for realizing any arithmetic function are AND, XOR and XNOR. These gate functions can be achieved with two transistors (excluding the inverters for complementary input signals) and their transistor level diagrams are shown in Figure 2.2.

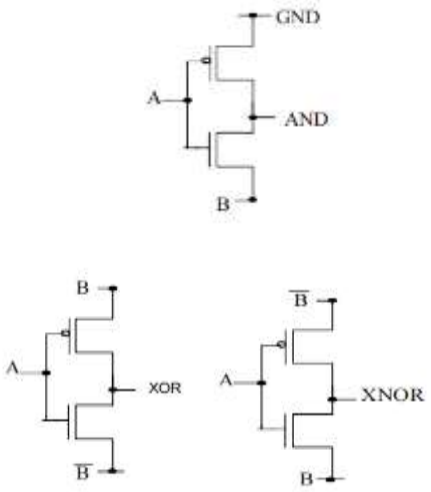


**Fig2 GDI Based Gates (a) AND (b) XOR (c) XNOR**

The operational characteristics of these gates are given in Table 2.2. Assume both the inputs have voltage swing, then the output voltages are subjected to different input combinations as given in Table 2.2.

| INPUT | | LOGIC GATE | | | |
|---|---|---|---|---|---|
| A | B | *AND* | *OR* | *XOR* | *XNOR* |
| '0' | '0' | $\lvert V_{tp}\rvert$ | $\lvert V_{tp}\rvert$ | $\lvert V_{tp}\rvert$ | $V_{DD}$ |
| '0' | '1' | $\lvert V_{tp}\rvert$ | $V_{DD}$ | $V_{DD}$ | $\lvert V_{tp}\rvert$ |
| '1' | '0' | *GND* | $V_{DD}$-$V_{tn}$ | $V_{DD}$-$V_{tn}$ | *GND* |
| '1' | '1' | $V_{DD}$-$V_{tn}$ | $V_{DD}$-$V_{tn}$ | *GND* | $V_{DD}$-$V_{tn}$ |

**Table2 Operational characteristics of gates using GDI logic**

**AND Gate:**

The transistor level diagram of the AND gate using GDI logic is shown in Figure 2.2 (a). The working mechanism of this gate is explained below:

Logic '0':

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For the input combinations AB = 00 and 01, NMOS transistor is switched OFF and PMOS transistor is switched ON. Therefore, the output is approximately equal to |Vtp| is obtained at the output, where Vtp is the threshold voltage of PMOS transistor. However, when AB = 10, the NMOS transistor becomes ON and PMOS transistor becomes OFF and passes ground potential (GND) at the output.

Logic '1':

When AB = 11, NMOS transistor is switched ON and PMOS transistor is switched OFF. Due to its operational characteristics it delivers poor '1' signal which is about VDD-Vtn at the output, Vtn denotes the threshold voltage of NMOS transistor

**XOR Gate:**

The transistor level diagram of the XOR gate using GDI logic is shown in Figure 2.2 (c). The working mechanism of this gate is explained below:

Logic '0':

When AB = 00, NMOS transistor is switched OFF and PMOS transistor is switched ON. Therefore, the output obtained is approximately equal to |Vtp|. However, when AB = 11, the NMOS transistor becomes ON and PMOS transistor becomes OFF and passes ground potential (GND) at the output.

Logic '1':

When AB = 01, PMOS transistor is switched ON and NMOS transistor is switched OFF. Therefore, VDD passes through PMOS transistor. On the contrary, the case occurs when AB = 10. In this case NMOS turns ON and PMOS turns OFF resulting in poor '1' signal in NMOS which is about VDD-Vtn at the output.

**XNOR Gate:**

The transistor level diagram of the XNOR gate using GDI logic is shown in Figure 2.2 (d). The working mechanism of this gate is explained below:

Logic '0':

When AB = 01, NMOS transistor is switched OFF and PMOS transistor is switched ON. Therefore, the output is approximately equal to|Vtp|. However, when AB = 10, the NMOS transistor becomes ON and PMOS transistor becomes OFF and passes ground potential (GND) at the output.

Logic '1':

When AB = 00, PMOS transistor is switched ON and NMOS transistor is switched OFF. Therefore, VDD passes through PMOS transistor.On the other hand, when AB = 10, NMOS turns ON and PMOS turns OFF resulting in poor '1' signal in NMOS which is about VDD-Vtn at the output.From this discussion, it is concluded that the output voltages are degraded by threshold voltage

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drop for certain input combinations. The reduction in output voltage increases significantly with increase in number of stages. Therefore, the design of full swing gates is necessary and it is discussed in the forthcoming subsections.

And finally the full adder is designed using the GDI based AND,XOR and XNOR gates

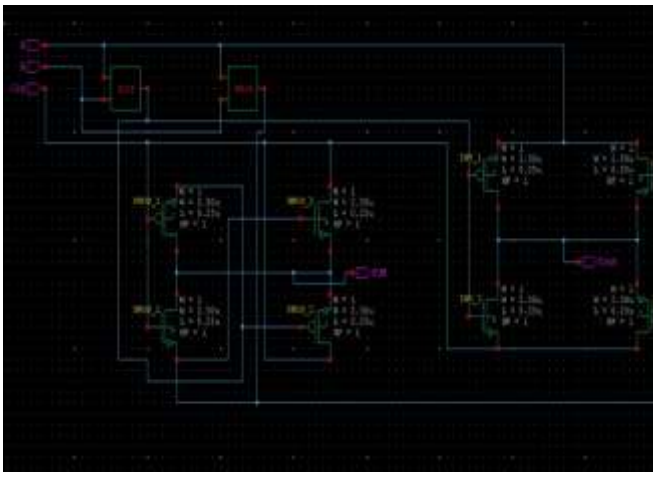

**Fig3 GDI Based Full Adder**

**Results**

The tool that is used to implement the power optimized 8 Bit Multiplier is TANNER EDA 13.0. Tanner tool is a Spice Computer Analysis Programmed for Analogue Integrated Circuits. Tannertool consists of the following Engine Machines: S-EDIT (Schematic Edit), T-EDIT (Simulation Edit), W-EDIT (Waveforms Edit), L-EDIT (Layout Edit). Using these engine tools, spice program provides facility to the use to design & simulate newideas in Analogue Integrated Circuits before going to the time consuming & costly process of chipfabrication.

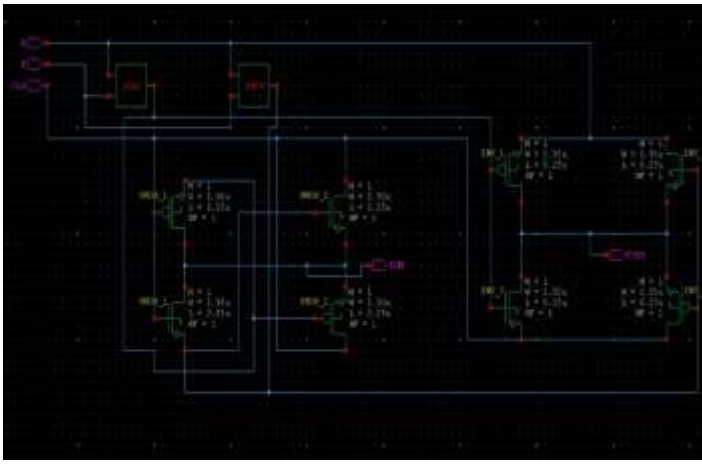

**Fig 4 RTL Schematic of Full Adder**

**The final 8 Bit Multiplier:**

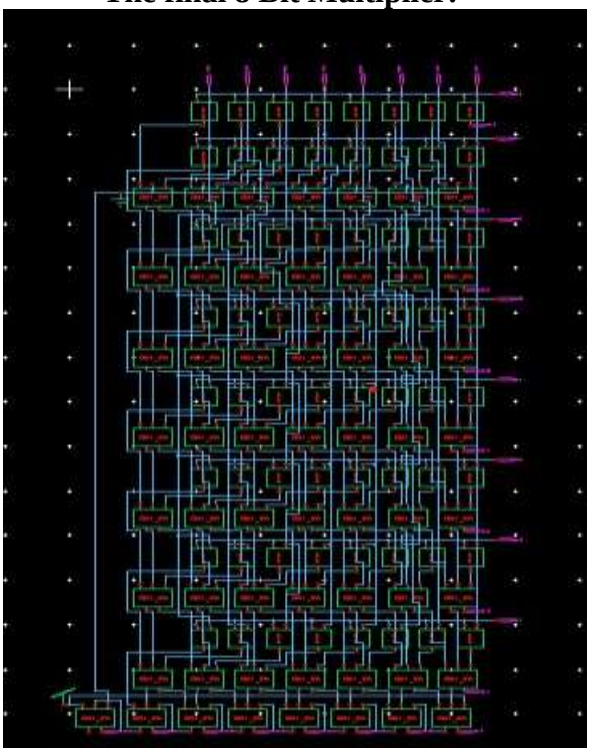

**Fig5 RTL Schematic of the 8 Bit Multiplier**

The final GDI Technique based 8 bit multiplier is developed using the AND Gates,and Full Adders which are developed using the Gate Diffusion Input(GDI) technique.The whole requirements of the multiplier are given to the multiplier using T spice tool.

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The simulation results of the proposed multiplier are compared with the existing multiplier implementation techniques .Table consists of the comparision in designing the required building blocks using CMOS technique and the same gates and adders designing using the Gate Diffusion Input(GDI) technique.

| S.No | Gates/Adders | Devices in CMOS technique | Devices in GDI technique |
|---|---|---|---|
| 1 | Inverter | 2 | 2 |
| 2 | AND Gate | 6 | 5 |
| 3 | XOR Gate | 12 | 4 |
| 4 | XNOR gate | 10 | 4 |
| 5 | Full Adder | 30 | 10 |

**Table 3 Number of devices required to implement basic gates and adders in CMOS and GDI logic Style**

The simulation results of the designed 8 bit multiplier design is compared with the existing techniques of different CMOS styles like Static CMOS logic,Complementary Pass transistor logic(CPL),Double Pass transistor logic(DPL),Domino Logic.

The comparitive analysis of the designed 8bit Multiplier with the different CMOS logic style implementation is done on the basis of Power consumption and Delay .Therefore Table 5.2 represents the comparitive analysis of the GDI technique multiplier with the different CMOS logic styles .

| S.No | Logic Styles | Power Consumption (uw) | Delay(ns) |
|---|---|---|---|
| 1 | Static CMOS Logic | 2.01 | 3.33 |
| 2 | Complementary Pass Transistor Logic | 14.93 | 1.43 |
| 3 | Double Pass transistor Logic | 10.39 | 1.82 |
| 4 | Domino Logic | 5.52 | 1.2 |
| 5 | Proposed Gate diffusion Input(GDI) Logic | 1.03 | 0.8 |

**Table 4 Performance Analysis of GDI technique 8 Bit multiplier :With CMOS Logic**

## CONCLUSION

The 8bit multiplier is implemented by using GDI Technique and Complementary Pass Transistor Logic. Implementation as well as simulations are compared and carried out in tanner Software showing less power consumption in GDI circuit. From the comparison table, it is clear that GDI based multipliers has least power consumption at 5volt supply compared to Complementary Pass

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Transistor Logic (CPL), Static CMOS, DPL, Domino logic. It is also most effective in terms of number of transistors required. Nowadays, chip area is very important parameter. With respect to chip area, GDI technique is significantly advantageous over other technique which cannot be calculated using tanner software. Calculation of area can be taken as future enhancement. There are many directions to extend the experiments presented in this thesis. The performance of multiplier can be investigated under signal processing transformation and so on applications such as filtering. Furthur power consumption can be reduced by using full swing technology.

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