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INVESTIGATION ON THE PERFORMANCE OF COMBINATIONAL CIRCUITS USING CHARGE SHARING DOMINO LOGIC

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Abstract
Domino logic is a CMOS based evaluation of dynamic logic techniques. Domino logic circuits are mainly used in high performance microprocessors and memories due to their superior speed and area characteristics as compared to static CMOS circuits. In Domino logic circuits the deviation of node voltage from nominal value due to charge-sharing leads to erroneous output. The pre_charge pulses in pre_charge phase are responsible for low noise immunity and extra power consumption. The paper proposes a new domino technique and shows improvement in charge sharing elimination, power consumption, delay, area, and speed. The simulation for conventional footed domino, literature-based domino techniques and proposed domino structure is performed using tanner EDA 250 nm technology at 2 V supply.The proposed design can be used for implementing high-speed digital circuits such as microprocessors and memories.
Keywords: Charge sharing; keeper; DOIND; TSPC; Power Consumption.

I. INTRODUCTION

Complementary Metal Oxide Semiconductors are widely used for variety of applications in VLSI field and became a logic style of choice for the digital semiconductor domain because of its low power consumption and ease of design with increased robustness. This became a major advantage of CMOS logic over the available manufacturing process, which suffers from flow of leakage currents or constant power dissipation and power consumption. The evaluation of various logic families like Static, pseudo NMOS, dynamic logics etc., which changes the ongoing market trend in manufacturing field, then speed and overhead area become the primary parameters of choice for fabrication industry that leads to invention of clocked logic styles named as Dynamic and Domino logics[1-4]. Static and Dynamic logics are different families of CMOS logic designs. In this project we are giving brief idea of some of domino logics and charge sharing issue in domino logic. To avoid the charge sharing issue a new domino technique is implemented using tanner software 250nm technology with 2V power supply.

1.1 STATIC CMOS LOGIC

Static cmos logic is designed by connecting a k-input pull up and k-input pull down network in series and output is taken from the common drain terminal at the junction of pull up and pull-down network. In this there will be more delay and more die area due to a greater number of transistors.

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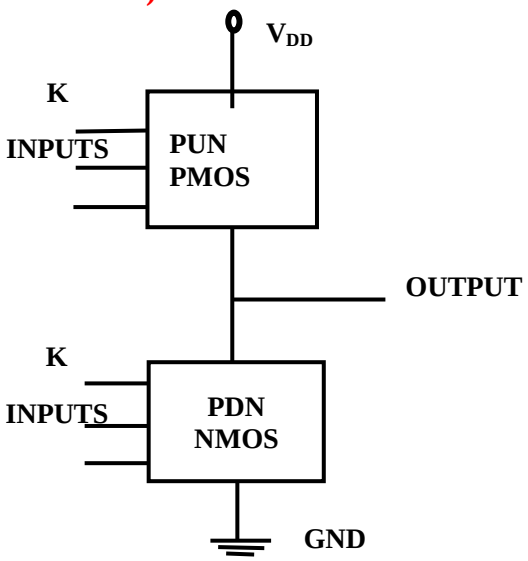

Fig1. Static CMOS Logic

1.2 DYNAMIC CMOS LOGIC

In this a single pmos transistor is used in pull up network, a pull-down network and a footer transistor or pass gate nmos transistor is used. In this number of transistors, circuit size and delay are also reduced. But when two or more dynamic logics [5-8] are cascaded, there will be cascading or false output issue [9].

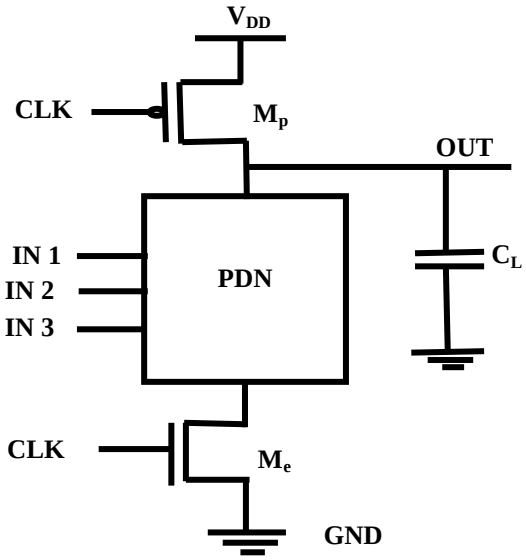

Fig2. Dynamic CMOS Logic

1.3 DOMINO LOGIC

Domino logic is implemented by connecting the dynamic logic in series with an inverter. This inverter provides a discharging path for the circuit. The domino logic operates in two phases namely pre_charge phase when clock is logic'0' and evaluation phase when clock is logic '1'

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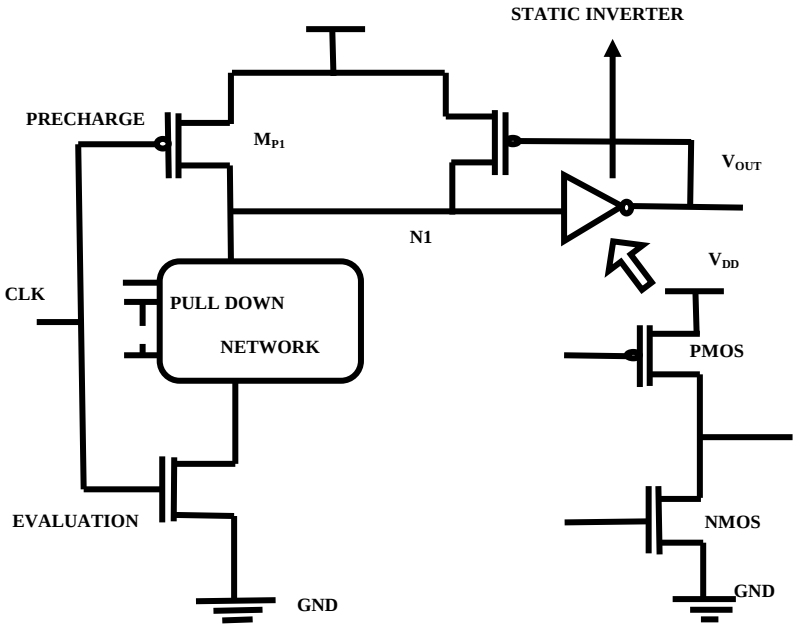

Fig3. Standard Domino Logic

II. LITERATURE BASED DOMINO LOGICS

The domino circuit is advantageous than the static and dynamic logics but to even decrease the power consumption and delay the domino circuits are modified as below.

2.1 PSEUDO DOMINO WITH STATIC BUFFER

Static buffer is the basic domino logic in this during the precharge phase irrespective of the input the dynamic node charges to VDD and is passed through an inverter so the output is low and when the circuit is in evaluation phase when input is low it maintains the precharge phase output and when input is high the charge at the dynamic node discharges to ground and output is high.

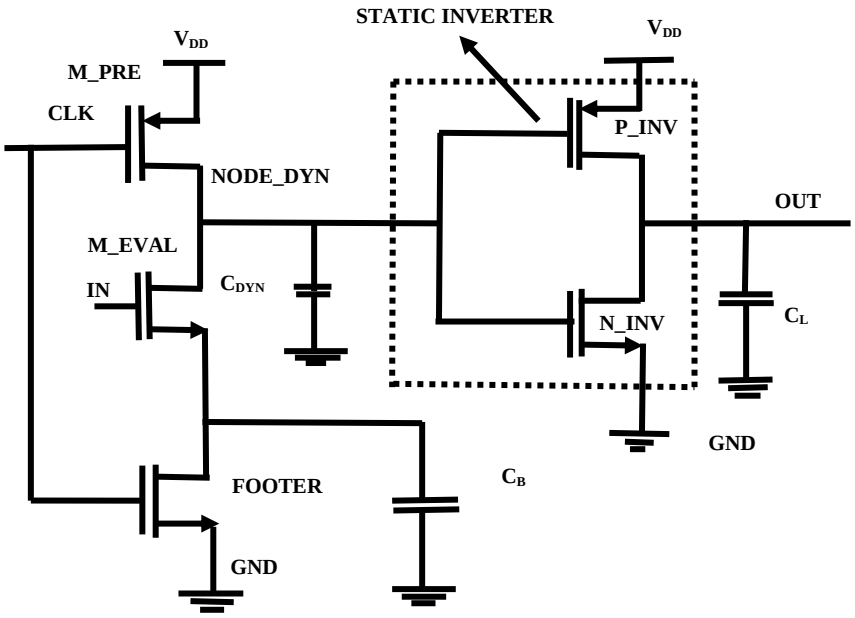

Fig4. Static Buffer

2.2 PSEUDO DOMINO BUFFER

This is implemented to overcome the drawbacks of static buffer. In this the source terminal of nmos of the inverter is connected to the drain of footer transistor. For this circuit when input is low irrespective of the phase the dynamic node charges to VDD. When the input is high during evaluation phase the charge at node dynamic discharges and the output becomes high. During precharge the nmos of the inverter is completely isolated and the output follows the evaluation phase.

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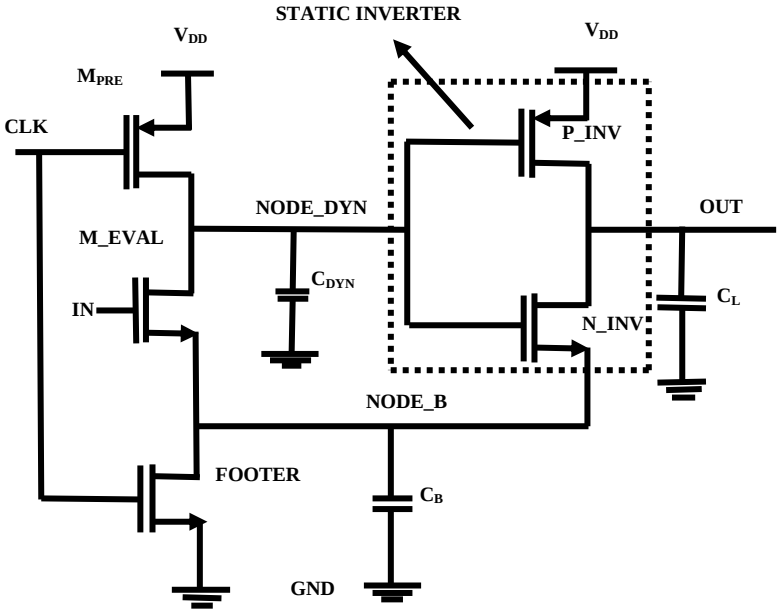

Fig5. Pseudo domino buffer

2.3 CDDK LOGIC

CDDK [11] is a clock delayed dual Keeper circuit. In this two weak pmos transistors are known as keeper transistors are used. During the precharge phase irrespective of the input the dynamic node charges and output is low. During the evaluation phase when input is low it follows the precharge phase and when the input is high the dynamic node discharges and the output becomes high.

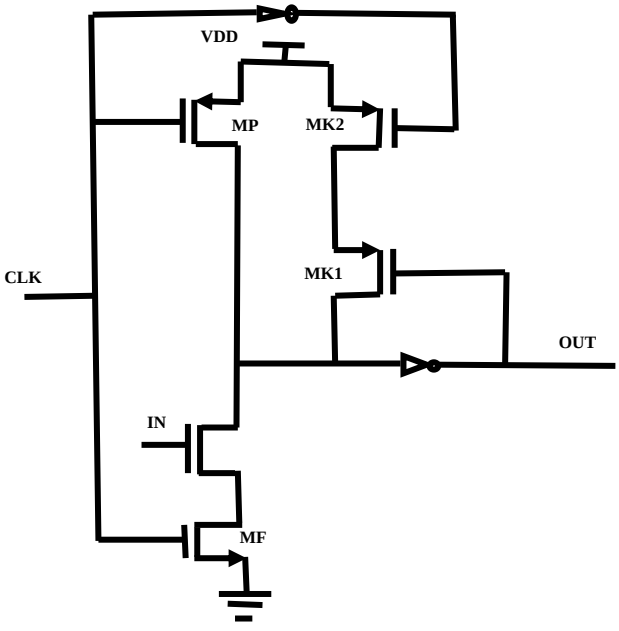

Fig6. CDDK Logic

2.4 DOIND LOGIC

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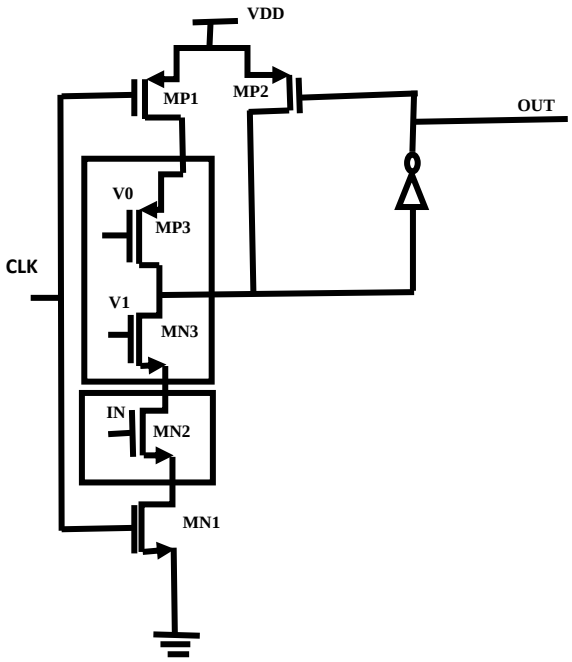

Fig7. DOIND Logic

DOIND [8] means dependent on input and clock. During precharge phase irrespective of the input the dynamic node charges and the output becomes low. During the evaluation phase when the input is low, the dynamic node charges and the output follows the precharge phase and when the input is high, the dynamic node discharges and output becomes high.

2.5 TSPC LOGIC

TSPC [11] is a domino logic implemented to overcome the drawbacks of conventional domino logics. When clock is high, evaluation transistor MNE and MS2 transistors are ON. Voltage at N_n node goes low and the transistors MLN moves near cut-off region of operation. Depending on logic inputs dynamic node voltage gets evaluated.

When clock is low, pre_charge PMOS transistor MPP gets ON, voltage at N_n is not sufficient to turn off transistor MLP, so it goes into cut-off region which allows conducting path to charge dynamic node. At the same time the gate to source voltage of transistor MNE1,MS2 become low therefore they are in OFF state. Thus, there is no discharging path exists for dynamic node to ground. Resistance of MLP is not high as OFF state resistance so it increases supply to ground path resistance and controls the leakage currents which reduce the power consumption.

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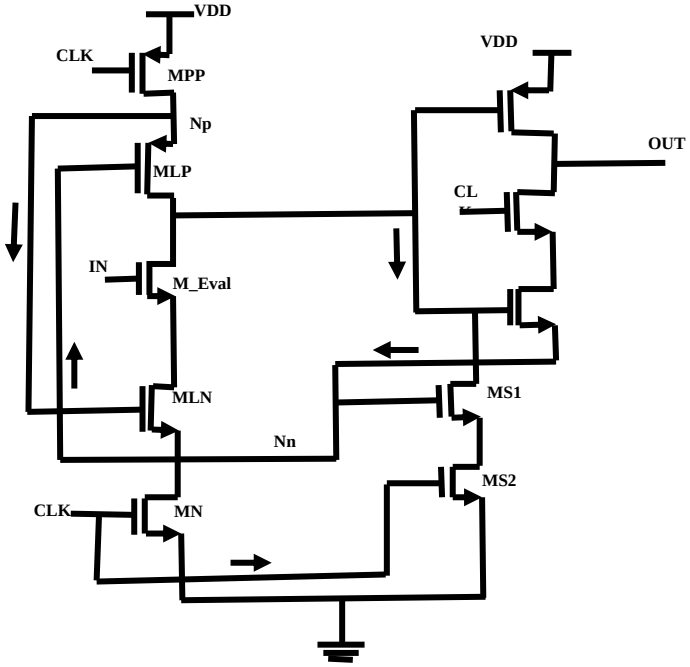

Fig8. TSPC Logic

III. PROPOSED DOMINO LOGIC

Domino logic have so many advantages like, it overcomes the cascading issues, uses less chip area, avoids glitches at output and increases speed due to reduction in load capacitance. But the few drawbacks which we observed in logics like conventional Pseudo Domino,DOIND,TSPC,CDDK logics is Charge Sharing issue when they are operating in evaluation phase. The way of eliminating the charge-sharing problem is to pre_charge internal nodes in the evaluation network along with dynamic node Node_dyn. Therefore, the weak PMOS transistor, known as keeper, is added to maintain the correct level at the output and allowing discharge path for dynamic node. We introduce a Pseudo Domino with inverted keeper [12] domino technique in order to reduce the charge sharing issue.

3.1 PSEUDO DOMINO WITH INVERTED KEEPER

The proposed domino structure-based buffer is shown in Fig 9.This is a circuit which overcomes the drawbacks of all the literature based domino techniques.. The circuit consists of two pre_charge transistors M1 and Mpre controlled by the output of the inverter “OUT” and CLK, respectively. In addition to footer transistors, four other transistors are employed (M2, M3, M4 and M5) for stacking effect in pre_charge phase. This will avoid connecting the source terminal of N_INV transistor to ground during pre_charge phase, which will reduce the output swing and hence save power in pseudo buffer design.

Irrespective of pre_charge or evaluation phase if applied input is low, then the M_Eval transistor is OFF, and the only current flowing through evaluation network is a sub threshold leakage current. This sub threshold leakage current increases the node voltage at Node_B slightly giving rise to increased body effect of the M_Eval transistor resulting in the increased threshold for evaluation network's transistor. Also, the gate to source (VGS) voltage of evaluation network transistor (here, M_Eval) reduces and becomes negative along with reduced drain-source voltage (VDS). Therefore, sub threshold current in the proposed circuit is reduced.

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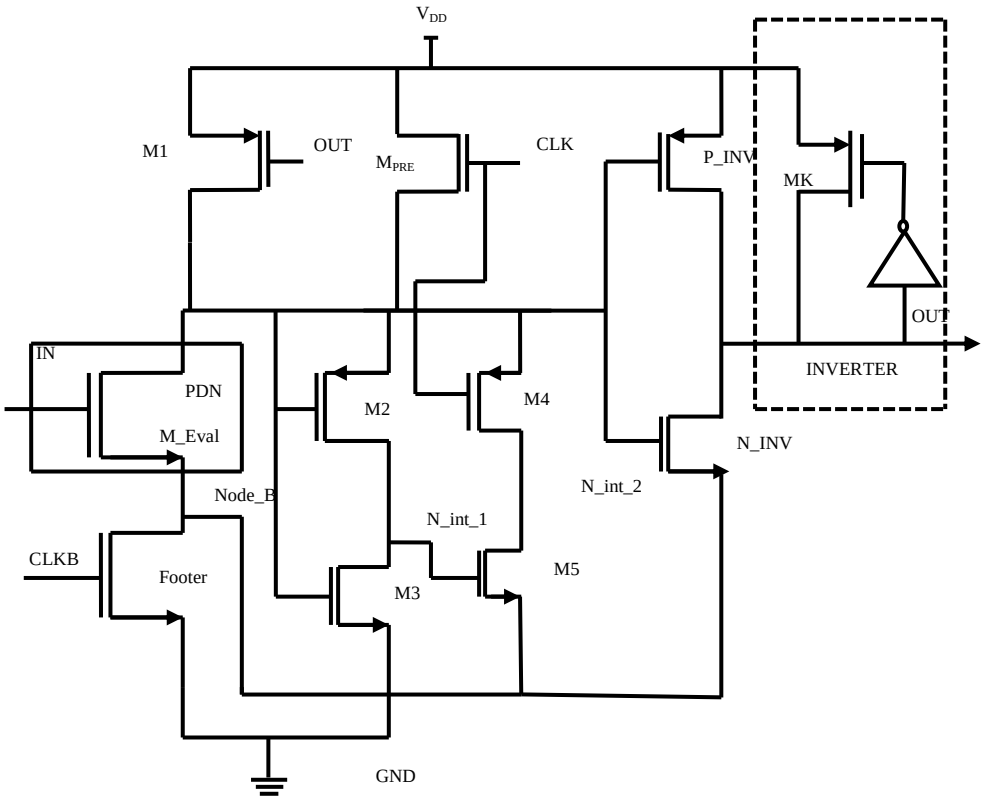

Fig9. Pseudo Domino with Inverted Keeper

IV. SIMULATION RESULTS

The simulation for conventional footed domino, literature-based domino techniques and proposed domino structure are performed using Tanner EDA 250 nm technology with a 2 V supply. Here, are the performance comparison between conventional footed, literature-based domino and proposed domino buffer is summed up in Table 1.

4.1: POWER AND DELAY COMPARISION ANALYSIS

The average power for the proposed circuit is least in comparison to other techniques. The delay of proposed domino is almost low when compared to all the literature-based techniques. Keeper circuits were introduced to maintain the dynamic node in the pre_charge phase while helping the output to overcome the voltage drop and maintain the correct level the output. The results indicate the power saved for the proposed circuit with respect to conventional, footed pseudo domino and literature-based domino logic due to less power dissipation. The range of power-saving with respect to conventional is higher and is between 87%. The power saving for proposed domino circuit compared with CDDK technique is between 71% and 75%. The range of power-saving with respect to DOIND technique is 40% to 45%. Although literature-based dominos are efficient in power saving compared with conventional domino, this saving is much less when compared with proposed domino-based circuits. It is because of the use of pseudo buffer at the output of the dynamic circuits. Finally Charge sharing issue is avoided by the use of keeper circuits at the dynamic node which always helps keeping Node_Dyn to high voltage.

Table 1: performance comparison of literature based and proposed domino technique

S.no	Logic name	Average power consumption(µW)	Delay(nsec)	Power delay product(fJ)
1	Conventional footed domino with static buffer	33	7	231

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2	Conventional footed domino with pseudo domino buffer	32	4	128
3	CDDK	14.81	3	44.43
4	DOIND	8.04	2.8	22.51
5	TSPC	7.01	2.5	17.52
6	Proposed pseudo domino with inverted keeper	4.78	0.9	4.302

4.2 PROPOSED DOMINO TECHNIQUE POWER, DELAY REPORT IN T-SPICE

The simulations for the proposed circuit like waveforms and Average Power Consumption and delay are analyzed using Tanner EDA generic 250nm software the power is obtained by adding a voltage source and specifying the start and stop times and delay is analyzed by expanding the waveforms obtained in T-Spice.Fig.10 shows the output waveforms of the proposed pseudo domino with inverted keeper. During the evaluation phase, CLK = 1 and CLKB = 0, pre_charge transistors M1, Mpre are established between evaluation network turning on of transistor M5, discharging Node_Dyn voltage from high to low, during pre_charge phase, CLK = 0 and CLKB = 1, pre_charge transistors M1 and Mpre both are turned ON maintaining the Node_Dyn high.

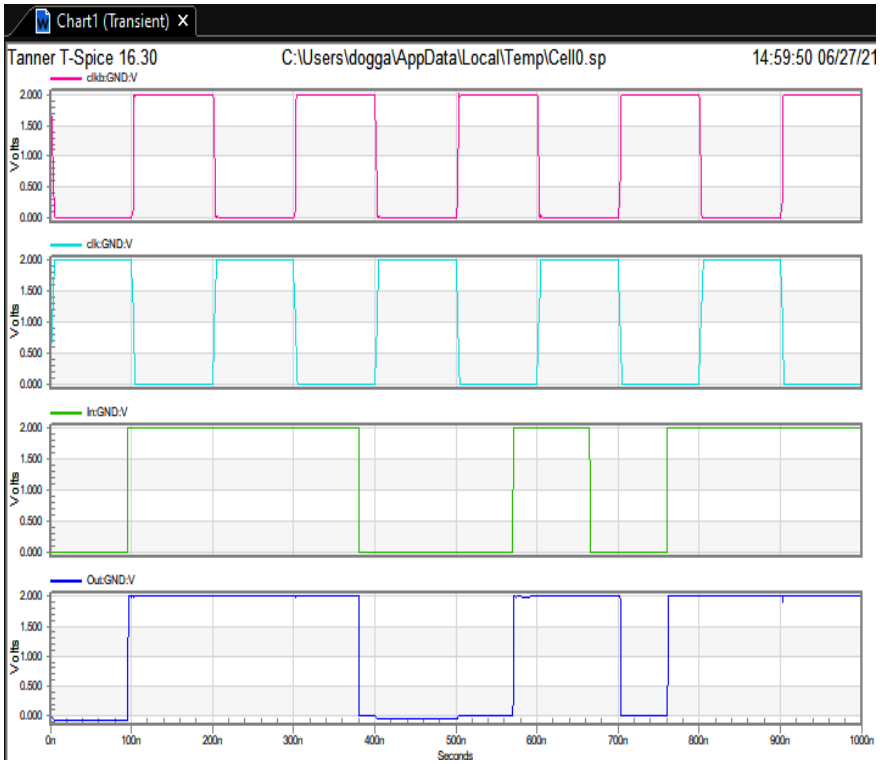

Fig10. Waveforms of Pseudo domino with inverted keeper

The power consumption report of proposed pseudo domino with inverted keeper is shown in fig11.It shows that this domino technique is having low power consumption when compared to all these previous literature based domino techniques. It is having maximum power consumption at time t=0.1 µsec which is shown in Tspice report which uses of 18 total number of devices in which 15 devices are active.

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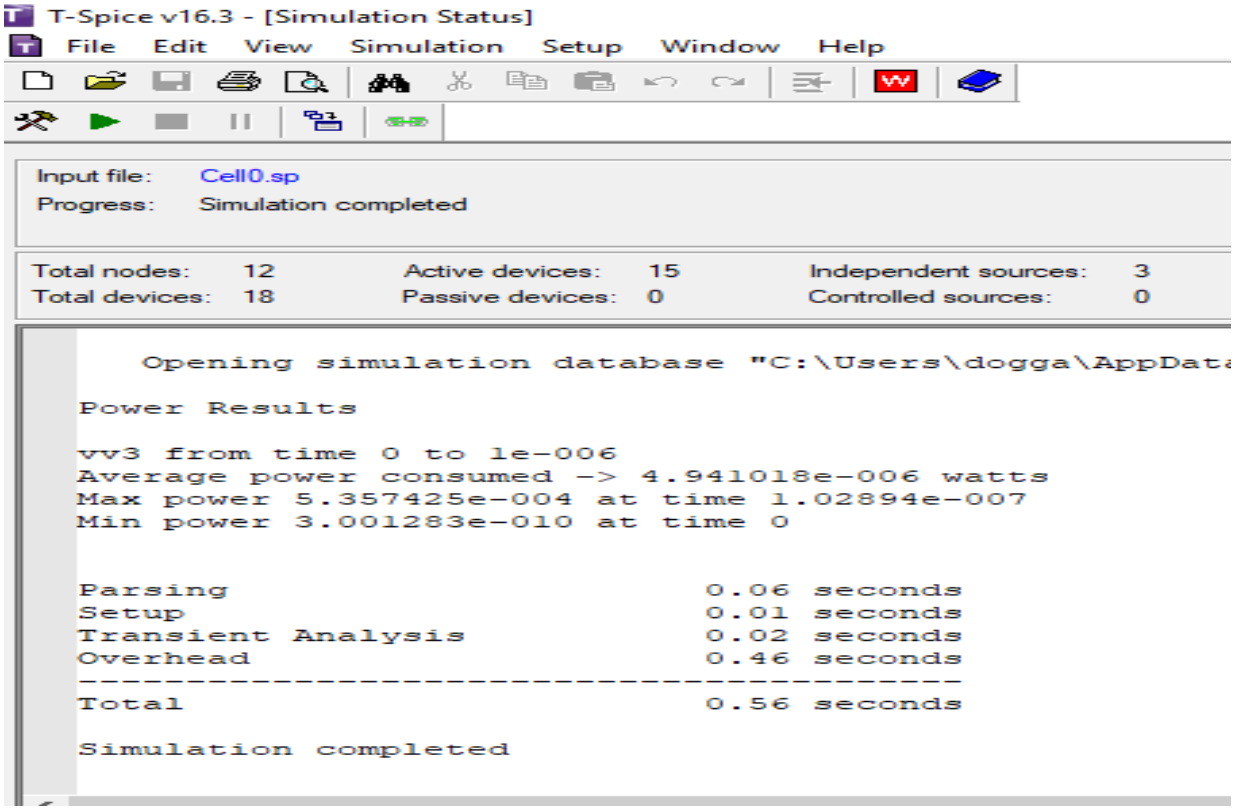

Fig11. Power Report of Pseudo domino with inverted keeper

Fig12. Shows the graphical representation of all the literature based domino techniques and proposed pseudo domino with inverted keeper. Conventional based domino logics are having the maximum power consumption when compared to CDDK, TSPC domino logics. The proposed domino logic is having power of 4.78µw and delay of 0.9 nsec.

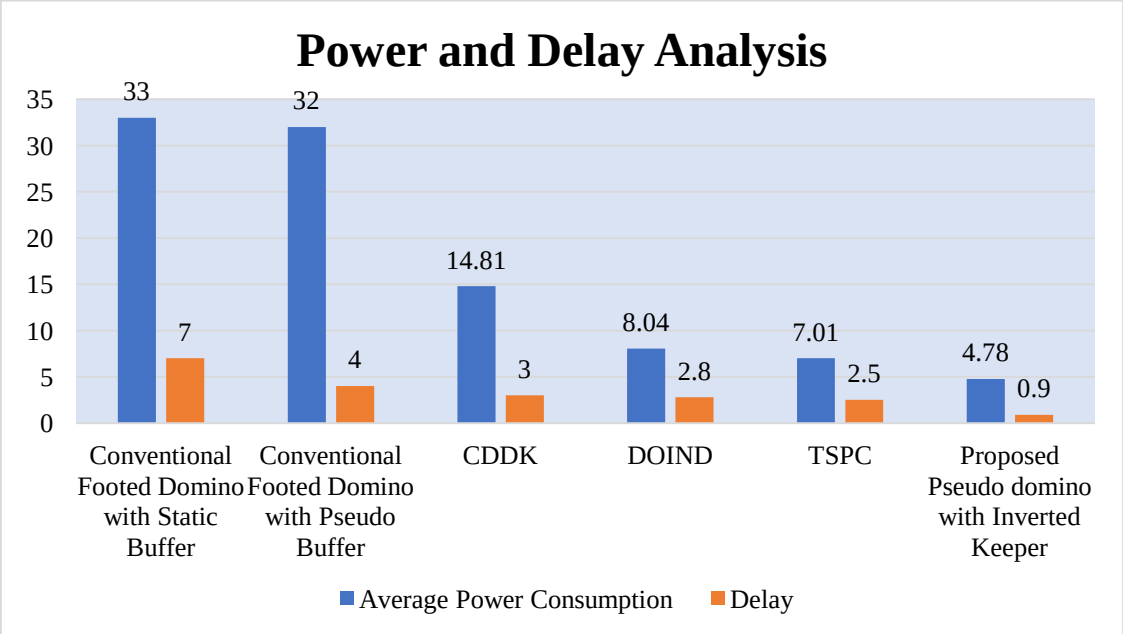

Fig12. Power and delay comparison of different domino techniques with proposed technique.

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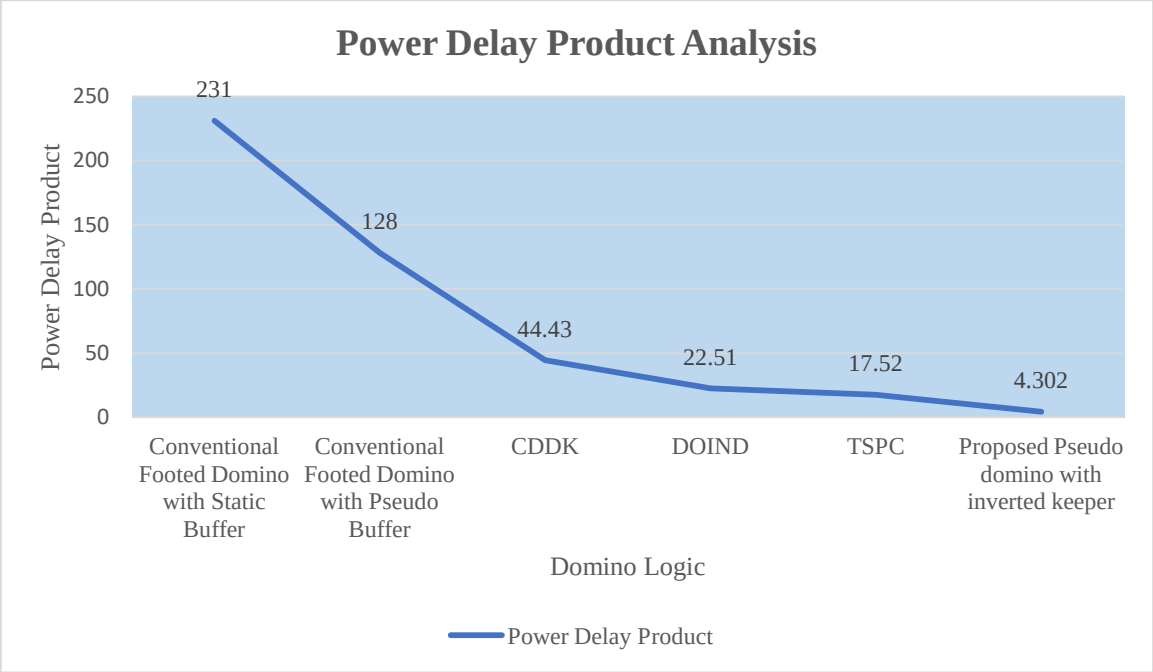

Fig13. Power delay product comparison of different domino techniques with proposed technique.

V CONCLUSION

Domino logic circuits are mainly used in high performance microprocessors and memories due to their superior speed and area characteristics, it overcomes the cascading issues, uses less chip area, avoids glitches at output and increases speed due to reduction in load capacitance and less number of transistors. But these logics suffer from charge sharing issue and performance degradation due to propagation of pre_charge pulses in pre_charge phase through static inverter buffer. In this project, a new DOMINO logic called Pseudo Domino with Inverted Keeper is proposed which is having low average power consumption of 4.8µW, less delay of 0.9nsec, and also due to less no transistors used, it occupies less die area. The range of power-saving with respect to conventional is higher and is between 87%. The power saving for proposed domino circuit compared with CDDK technique is between 71% and 75%. The range of power-saving with respect to DOIND technique is 40% to 45%. It overcomes the charge sharing issue by using PMOS keeper transistors. These keeper transistors make the dynamic node voltage always charging to V_{DD} without losing any charge. Therefore, this Pseudo domino with inverted keeper domino technique which overcomes the Charge sharing issue that was observed in all the existing domino logics. It works faster than all the existing domino logics. Finally, this project concludes with proposed Pseudo domino with inverted keeper technique which is having low power consumption and delay.

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