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APPLICATION OF ADAPTIVE HOLD LOGIC FOR IMPLEMENTING AGING-AWARE RELIABLE MULTIPLIER

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Abstract— In this paper proposed a Digital multipliers are among the most critical arithmetic functional units. The overall performance of these systems depends on the throughput of the multiplier. Meanwhile, the negative bias temperature instability effect occurs when a pMOS transistor is under negative bias (Vgs = −Vdd), increasing the threshold voltage of the pMOS transistor, and reducing multiplier speed. A similar phenomenon, positive bias temperature instability, occurs when an nMOS transistor is under positive bias. Both effects degrade transistor speed, and in the long term, the system may fail due to timing violations.Therefore, it is important to design reliable high-performance multipliers. In this paper, we propose an aging-aware multiplier design with a novel adaptive hold logic (AHL) circuit. The multiplier is able to provide higher throughput through the variable latency and can adjust the AHL circuit to mitigate performance degradation that is due to the aging effect. Moreover, the proposed architecture can be applied to a column- or row-bypassing multiplier. The experimental results show that our proposed architecture with 16 ×16 and 32 ×32 column-bypassing multipliers can attain up to 62.88% and 76.28% performance improvement, respectively, compared with 16×16 and 32×32 fixed-latency column bypassing multipliers. Furthermore, our proposed architecture with 16 × 16 and 32 × 32 row-bypassing multipliers can achieve up to 80.17% and 69.40% performance improvement as compared with 16×16 and 32 × 32 fixed-latency row-bypassing multipliers.

Keywords: Adaptive hold logic (AHL), negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), reliable multiplier, variable latency.

INTRODUCTION

In this project, we propose an aging-aware reliable multiplier design with novel adaptive

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hold logic (AHL) circuit. The multiplier is based on the variable-latency technique and can adjust the AHL circuit to achieve reliable operation under the influence of NBTI and PBTI effects. To be specific, the contributions of this paper are summarized as follows: 1) novel variable-latency multiplier architecture with an AHL circuit. The AHL circuit can decide whether the input patterns require one or two cycles and can adjust the judging criteria to ensure that there is minimum performance degradation after considerable aging occurs; 2) comprehensive analysis and comparison of the multiplier's performance under different cycle periods to show the effectiveness of our proposed architecture; 3) an aging-aware reliable multiplier design method that is suitable for large multipliers. We implemented the 4x4 and 8x8 bypassing multipliers.

- Adaptive hold logic (AHL) circuit

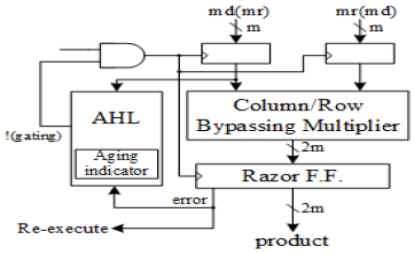

Fig1: Proposed Architecture

PROBLEM STATEMENT

Digital world multipliers are the most critical arithmetic functional units. The overall performance of these systems depends on the throughput of the multiplier. Meanwhile, the negative bias temperature instability effect occurs when a pMOS transistor is under negative bias increasing the threshold voltage of the pMOS transistor, and reducing multiplier speed. A similar phenomenon, positive bias temperature instability, occurs when an nMOS transistor is under positive bias. Both effects degrade transistor speed, and in the long term, the system may fail due to timing violations. Therefore, it is important to design reliable high-performance multiplier.

LITERATURE REVIEW

1: Bipul C Paul, Kunhyuk Kang, Haldun Kufluoglu,

With the rapid progress in semiconductor technology and the shrinking of device geometries, the resulting processors are increasingly becoming prone to effects like aging and soft errors. As a processor ages, its electrical characteristics degrade, i.e., the switching times of its transistors increase. Hence, the processor cannot continue error-free operation at the same clock frequency and/or voltage for which it was originally designed. In order to mitigate such effects, recent research proposes to equip processors with special circuitry that automatically adapts its clock frequency in response to changes in its circuit-level timing properties. From the point of view of tasks running on these

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processors, such autonomic frequency scaling (AFS) processors become slower as they gradually age. This leads to additional execution delay for tasks, which needs to be analyzed carefully, particularly in the context of hard real time or safety-critical systems.

2. Alejandro Masrur, Philipp Kindt, Martin Becker and Samarjit Chakraborty

Design of portable battery operated multimedia devices requires energy efficient multiplication circuits. This paper presents a novel approach to reduce power consumption of digital multiplier based on dynamic bypassing of partial products. The bypassing elements incorporated into the multiplier hardware eliminates the redundant signal transitions, which appear within the carry save adders when the partial product is zero.

PROPOSED AGING-AWARE MULTIPLIER

The proposed aging-aware reliable multiplier design. It introduces the overall architecture and the functions of each component and also describes how to design AHL that adjusts the circuit when significant aging occurs.

Proposed Architecture

Proposed aging-aware multiplier architecture, which includes two *m*-bit inputs (*m* is a positive number), one 2*m*-bit output, one column- or row-bypassing multiplier, 2*m* 1-bit Razor flip-flops, and an AHL circuit.

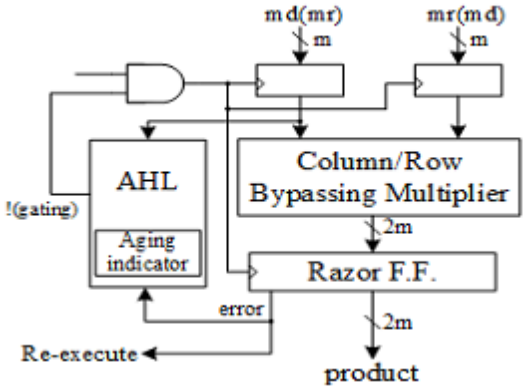

Fig2: Proposed architecture (md means multiplicand; mr means multiplicator).

Hence, the two aging-aware multipliers can be implemented using similar architecture, and the difference between the two bypassing multipliers lies in the input signals of the AHL. According to the bypassing selection in the column or rowbypassing multiplier, the input signal of the AHL in the architecture with the column-bypassing multiplier is the multiplicand, whereas of the row-bypassing multiplier is the multiplicator.

SIMULATION IMPLEMENTATION

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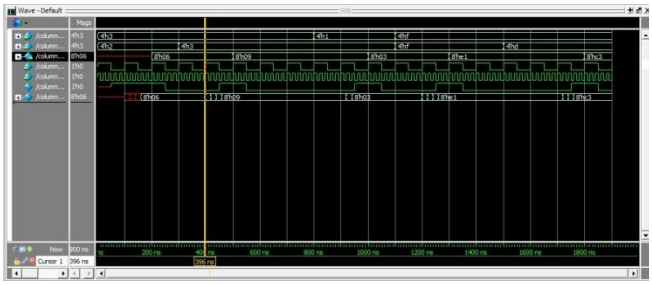
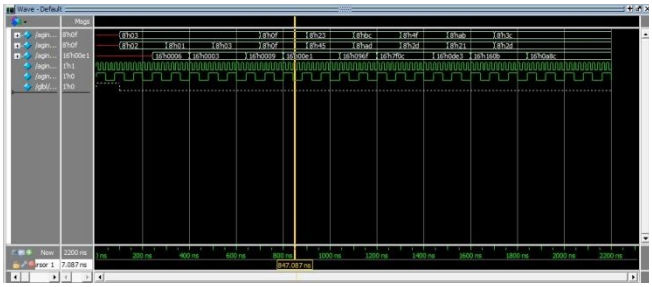
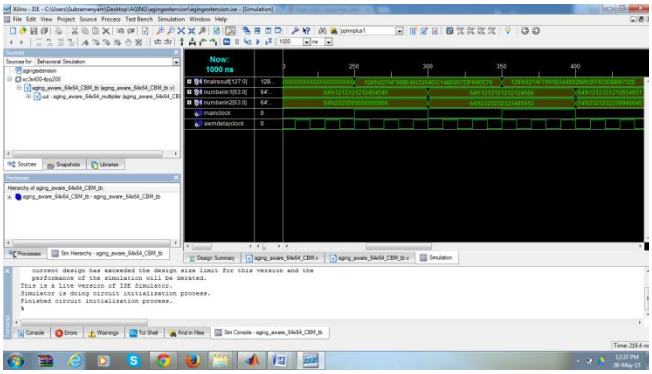


aging_aware_4x4_rbm_multiplier



aging_aware_8x8_extension_rbm_multiplie r



CONCLUSION

In this paper, In Proposed the multiplier is based on the variable-latency technique. The AHL circuit to achieve reliable operation under the influence of NBTI and PBTI effects. Our proposed architecture with the 8x8 column-bypassing multipliers and row-bypassing multipliers. We are using Razor flip flop to hold the logic. And the output of this is given as an input to the aging indicator.

Note that in addition to the BTI effect that increases transistor delay, interconnect also has its aging issue, which is called electro migration. Electro migration occurs when the current density is high enough to cause the drift of metal ions along the direction of electron flow. The metal atoms will be gradually displaced after a period of time, and the geometry of the wires will change. If a wire becomes narrower, the resistance and delay of the wire will be increased, and in the end, electro migration may lead to open circuits. This issue is also more serious in advanced process technology because metal wires are narrower, and changes in the wire width will cause larger resistance differences. If the aging effects caused by the BTI effect and electro migration are considered together, the delay and performance degradation will be more significant. Fortunately, our proposed variable latency multipliers can be used under the influence of both the BTI effect and electro migration. In addition, our proposed variable latency multipliers have less performance degradation because variable latency multipliers have less timing waste, but traditional multipliers need to consider the degradation caused by both the BTI effect and electro migration and use the worst case delay as the cycle period..

FUTURE SCOPE:

In future, we can implement more bit sized multiplier with even lesser delay by using the

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parallel prefix adders inside the multipliers instead of normal carry select adders.

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Vol-11 Issue-01 2021

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