ISSN: 2278-4632
Vol-11 Issue-01 2021

Design_of_Efficient_32-bit_Vedic_Multiplier

Binni Gollapalli, PG Scholar, Department of ECE, Vikas Group of Institutions, JNTUK, Andhra Pradesh, Email id: binnigollapalli23@gmail.com

G Sekhar Reddy, Assistant Prof, Department of ECE, Vikas Group of Institutions, JNTUK, Andhra Pradesh, Email id: gaddamsekharreddy@gmail.com

Abstract: Multipliers are vital components of any processor or computing machine. More often than not, performance of microcontrollers and Digital signal processors are evaluatedon the basis of number of multiplications performed in unit time. Hence better multiplier architectures are bound to increase the efficiency of the system. Vedic multiplier is one such promising solution. Its simple architecture coupled with increased speed forms an unparalleled combination for serving any complex multiplication computations. Tagged with these highlights, implementing this with reversible logic further reduces power dissipation Power dissipation is another important constraint in an embedded system which cannot be neglected.

In this paper we bring out a Vedic multiplier known as "Urdhva Tiryakbhayam" meaning vertical and crosswise, implemented using reversible logic, which is the first of its kind. This multiplier may find applications in Fast Fourier Transforms (FFTs), and other applications of DSP like imaging, software defined radios, wireless communications.For arithmetic multiplication, various Vedic multiplication techniques like Urdhva tiryakbhyam, Nikhilam and Anurupye has been thoroughly discussed. It has been found that Urdhva tiryakbhyam Sutra is most efficient Sutra (Algorithm), giving minimum delay formultiplication of all types of numbers, either small or large.Further, the Verilog HDL coding of Urdhva tiryakbhyam Sutra for 8x8 bits multiplication and their FPGA implementation by Xilinx Synthesis Tool on Spartan 3E kit have been done.

Keywords- Urdhva Tiryakbhayam,Fast Fourier Transforms (FFTs),Vedic multiplier..

1.Introduction: A Multiplier is an electronic circuit used in digital circuits, such as a computer, to multiply two binary numbers. It is built using binary adders. A variety of computer arithmetic techniques can be used to implement a digital multiplier. In digital circuits multiplying to binary numbers is done using repeated addition using full adders and half adders. A multiplier is used in many applications such as image processing, signal processing, microprocessors, and microcontrollers, etc.

ISSN: 2278-4632
Vol-11 Issue-01 2021

There are many types of multipliers such as array multiplier, Wallace tree multiplier, Vedic multiplier, booth multiplier, among all these multipliers Vedic multiplier has less delay when compared to other multipliers [2].Vedic Multiplier is an efficient multiplier with less delay. The structure/block diagram of the Vedic multiplier is similar to that of the array multiplier with some changes in the most significant bit. Vedic Multiplier is based on 16 Vedic sutras in which Urdhva triyakbhyam is general multiplication formula. The Urdhva triyakbhyam sutra is also known as vertical and crosswire. This sutra was traditionally used in ancient India for multiplication in less time. As the number of multiplication bits increases the timing delay also increases. The Vedic multiplier is used in various applications such as digital signal processing (DSP), communication systems. It is also used in image Processing as fast Fourier transforms, convolution, and in an ALU of a microprocessor.

2.Vedic Multiplier: Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya-Veda (book on civil engineering and architecture), this is an upa-veda (supplement) of Atharvana Veda. It covers explanation of several modern mathematical terms including quadratic equations, factorization ,arithmetic, geometry (plane, co- ordinate), trigonometry, and even calculus. The proposed Vedic multiplier is based on the Vedic multiplication formulae (Sutras). For the multiplication of two numbers in the decimal number system the proposed Sutras have been traditionally used. To make the proposed algorithm compatible with the digital hardware in this work, the same ideas are applied to the binary number system.

Urdhva Tiryakbhyam Sutra is applicable to all cases of multiplication. This sutra performs the multiplication using the principle Vertically and crosswise multiplication. The generation of all partial products can be done with the concurrent addition of these partial products. The figure explains parallelism in generation of partial products and their summation.

The algorithm can be generalized for n x n bit number. This multiplier is independent of the clock frequency of the processor as the partial products and their sums are calculated in parallel. The same amount of time will require by this multiplierto calculate the product and thus it is independent of the clock frequency.

ISSN: 2278-4632
Vol-11 Issue-01 2021

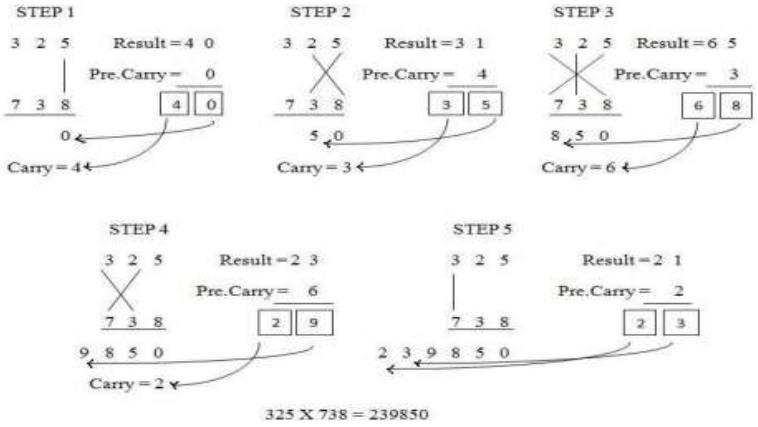

Fig1: Showing Multiplication of two decimal numbers by UrdhvaTiryakbhyam

Algorithm for 4 x 4 bit Vedic multiplier Using Urdhva Tiryakbhyam (Vertically and crosswise) for two Binary numbers

CP = Cross Product (Vertically and Crosswise)

X3 X2 X1X0 Multiplic andMultiplier
Y3 Y2 Y1Y0

H G F E D C BA

P7 P6 P5 P4 P3 P2 P1P0 Product

PARALLEL COMPUTATION METHODOLOGY

CP X0 = X0 * Y0 = AY0

2. CP X1 X0 = X1 * Y0+X0 * Y1 = BY1 Y0
3. CP X2 X1 X0 = X2 * Y0 +X0 * Y2 +X1 * Y1 = CY2
   Y1 Y0
4. CP X3 X2 X1 X0 = X3 * Y0 +X0 * Y3+X2 * Y1 +X1 * Y2 = DY3
   Y2 Y1 Y0

5. CP X3 X2 X1 = X3 * Y1+X1 * Y3+X2 * Y2 = EY3
   Y2 Y1

ISSN: 2278-4632
Vol-11 Issue-01 2021

6. CP X3 X2 = X3 * Y2+X2 * Y3 = F Y3
Y2

7 CP X3 = X3 * Y3 = GY3

3 Results

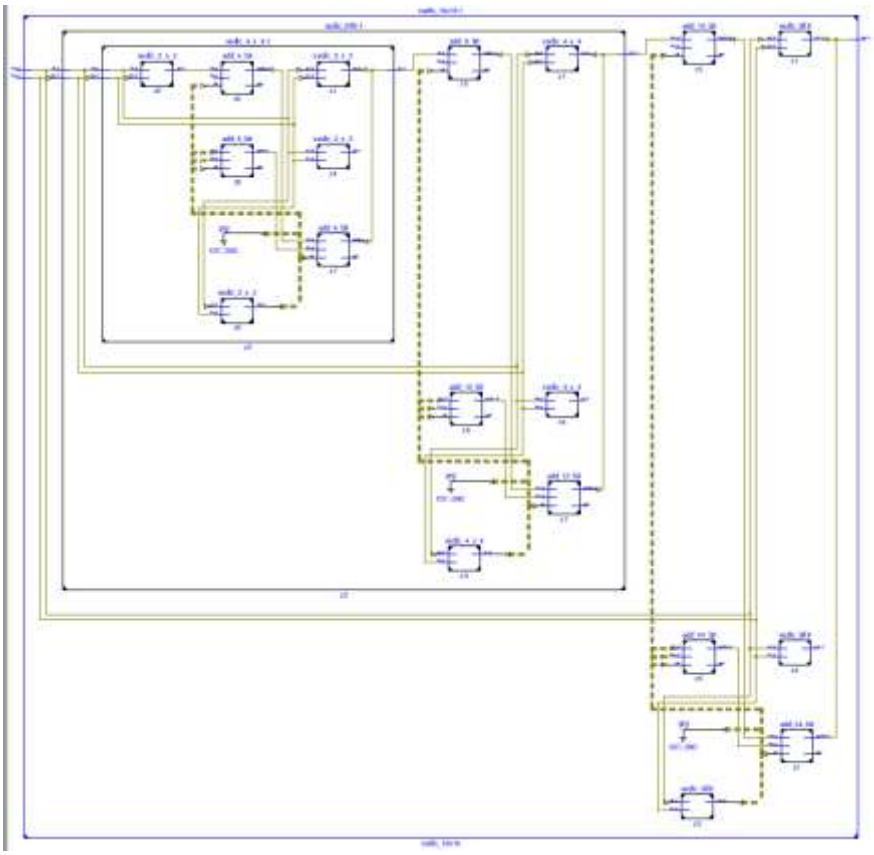

Fig 1 RTL Schematic 32*32 bit vedic multiplier

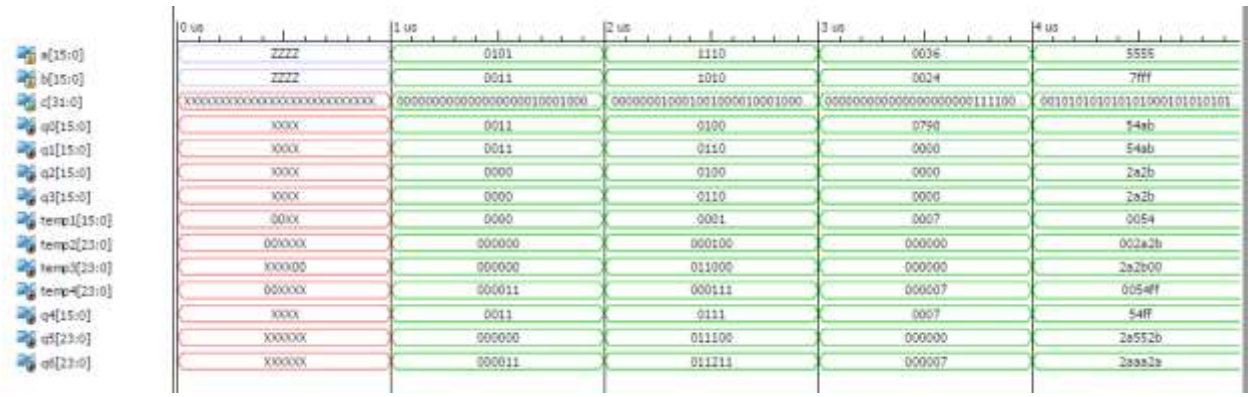

Fig 2 Simulation results

ISSN: 2278-4632
Vol-11 Issue-01 2021

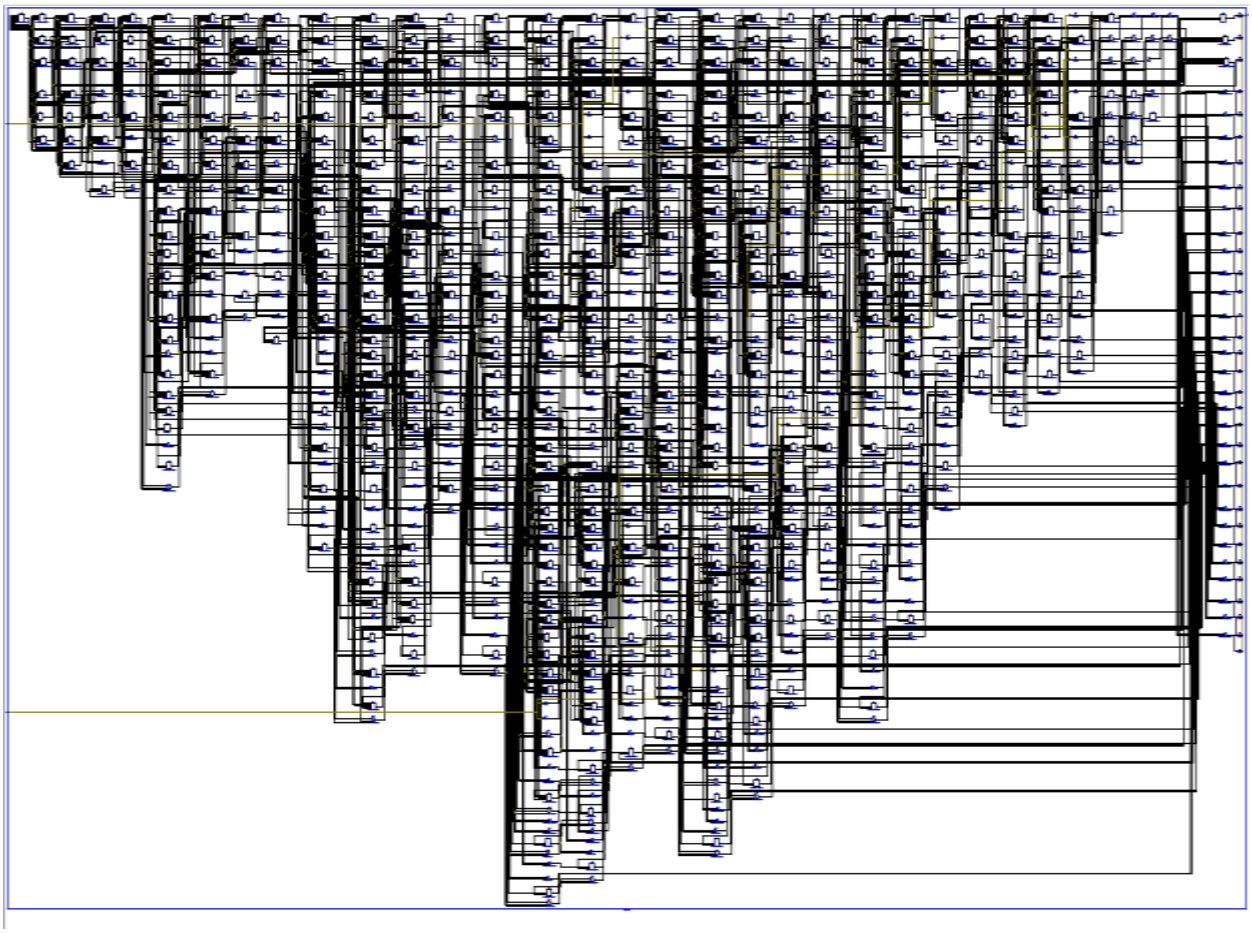

Fig 3 Technology Schematic

4 Conclusion and Further Scope

Urdhva tiryakbhyam sutram, Nikhilam sutram and Anurupyena sutram are the important among such vedic algorithms which can reduce the delay, power and hardwarerequirements for multiplication of numbers. The hardware realization of the Vedic mathematics algorithms is easily possible through the FPGA implementation of these multipliers. The computational speed drastically reduces if all those methods are effectively used for the hardware implementation. Hence there is a chance for implementing a complete ALU using Vedic mathematics methods. Vedic mathematics is long been known but has not been implemented in the DSP and ADSP processors employing large number of

ISSN: 2278-4632
Vol-11 Issue-01 2021

multiplications in calculating the various transforms like FFTs and the IFFTs. By using these ancient Indian Vedic mathematics methods world can achieve newheights of performance and quality for the cutting edge technology devic

REFERENCES

1. Swami Bharati Krishna Tirthaji Maharaja, "Vedic Mathematics", MotilalBanarsidass Publishers, 1965.
2. Rakshith T R and RakshithSaligram, "Design of High Speed Low Power Multiplier using Reversible logic: a Vedic Mathematical Approach", International Conference on Circuits, Power and Computing Technologies (ICCPCT-2013), ISBN: 978-1-4673-4922-2/13, pp.775-781.
3. M.E. Paramasivam and Dr. R.S. Sabeenian, "An Efficient Bit Reduction Binary Multiplication Algorithm using Vedic Methods", IEEE 2nd International Advance Computing Conference, 2010, ISBN: 978-1-4244-4791-6/10, pp. 25-28.
4. Sushma R. Huddar, Sudhir Rao Rupanagudi, Kalpana M and Surabhi Mohan, "Novel High Speed Vedic Mathematics Multiplier using Compressors", International Multi conference on Automation, Computing, Communication, Control and Compressed Sensing(iMac4s), 22-23 March 2013, Kottayam, ISBN: 978-1-4673-5090-7/13, pp.465- 469.
5. L. Sriraman and T. N. Prabakar, "Design and Implementation of Two Variables Multiplier Using KCM and Vedic Mathematics", 1st International Conference on Recent Advances in Information Technology (RAIT -2012), ISBN: 978-1-4577-0697-4/12.
6. Prabir Saha, Arindam Banerjee, Partha Bhattacharyya and Anup Dandapat, "High Speed ASIC Design of Complex Multiplier Using Vedic Mathematics", Proceeding of the 2011 IEEE Students' Technology Symposium 14-16 January,2011, IIT Kharagpur, ISBN: 978-1-4244-8943-5/11, pp.237-241.
7. Soma BhanuTej, "Vedic Algorithms to develop green chips for future", International Journal of Systems, Algorithms & Applications, Volume 2, Issue ICAEM12, February 2012, ISSN Online: 2277-2677.
8. Yogendra and Anil Kumar Gupta," Design of High Performance 8-bit Vedic Multiplier", International Conference on Advances in Computing, Communication, & Automation (ICACCA), September 2016.

ISSN: 2278-4632
Vol-11 Issue-01 2021

9. S. Jayakumar and S. Sumathi, “High – Speed Vedic Multiplier for Image Processing using FGPA,” IEEE/10th International Conference on Intelligent Systems and Control (ISCO), January 2016.
10. Rendlesham Gupta, Rajdeep Shar, K. L. Baishnab Jishan Mehedi, “Design of high performance 8-bit Vedic Multiplier using compressor,” IEEE/International Conference on Advances in Engineering and Technology (ICAET), May 2014.
11. J. Vinoth Kumar and C. Kumar Charlie Paul., “Design of Modified Vedic Multiplier and FPGA implementation in Multilevel 2d-DWT for Image Processing Applications,” Second International Conference on Current Trends in Engineering and Technology - ICCTET 2014, July 2014.
12. Vaidyanathan Kuchai, Linganagouda Kulkarni, Subhash Kulkarni, “High Speed and Area Efficient Vedic Multiplier,” International Conference on Devices, Circuits and Systems (ICDCS), April 2012

Binni Gollapall, Pg scholar, Vikas Group of Institutions, JNTUK, Andhra Pradesh, Specialization in VLSI Design

G SEKHAR REDDY, M.TECH IN GITAM UNIVERSITY, ASSISTANT PROF, AREA OF INTEREST :LOW POWER VLSI, Vikas Group of Institutions, JNTUK, Andhra Pradesh